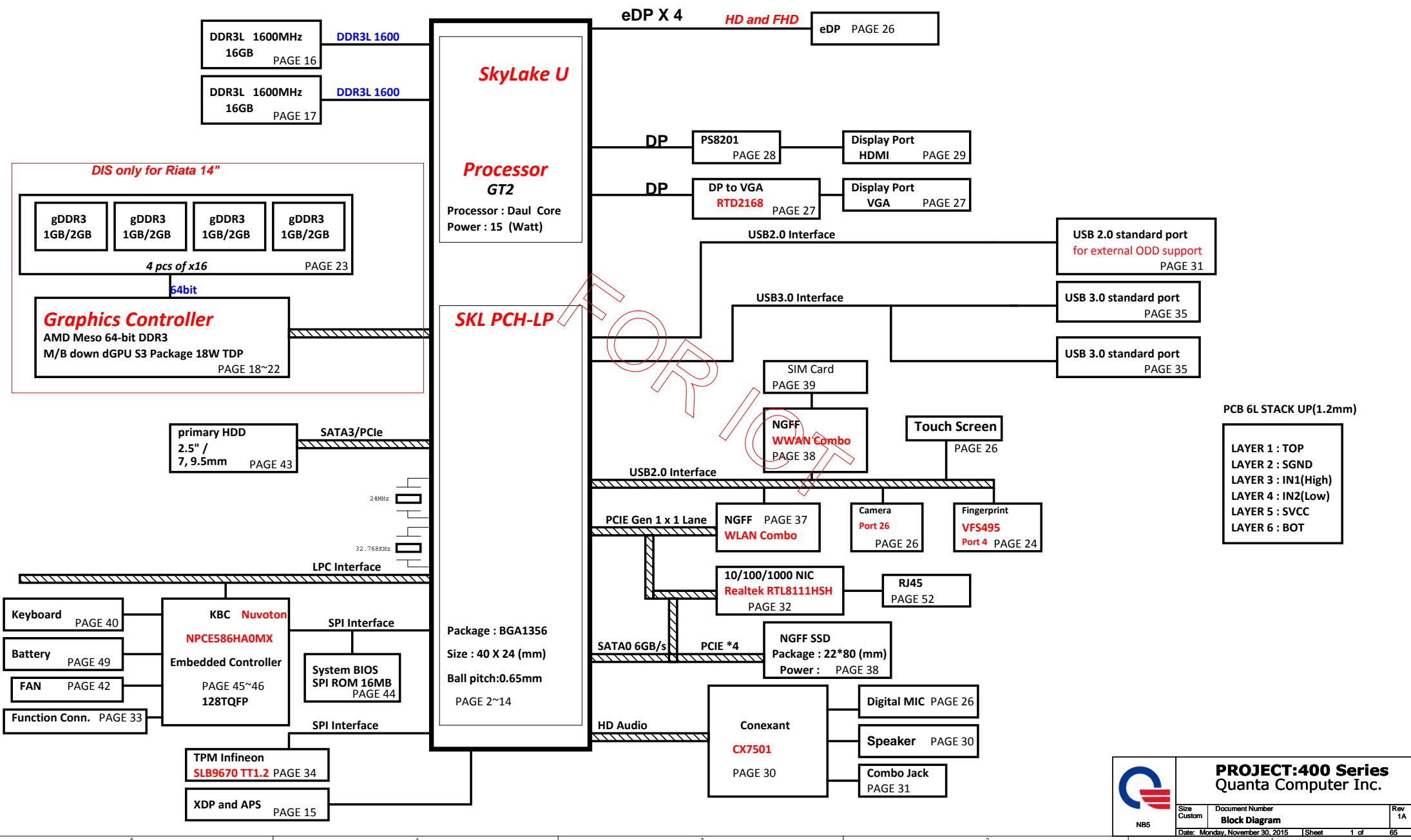
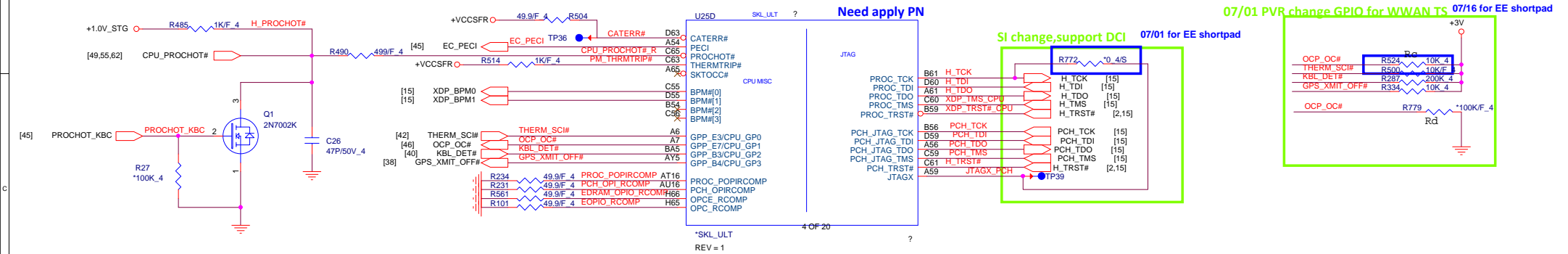
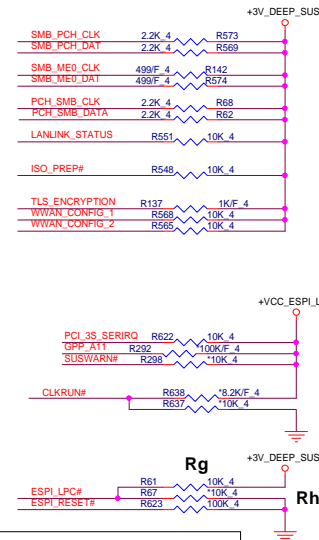
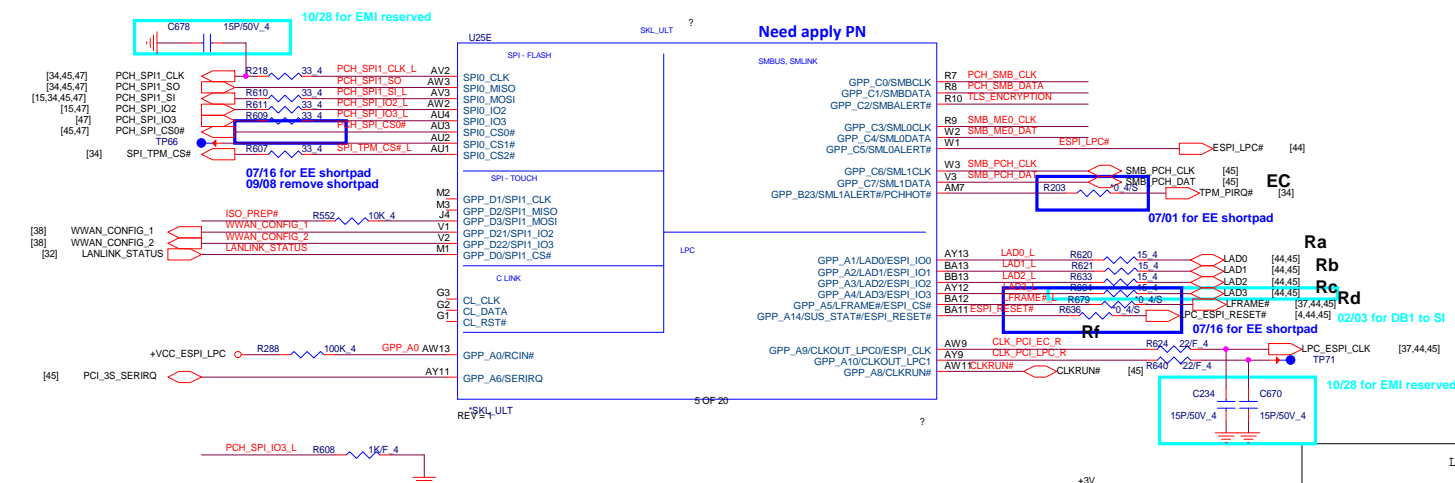


Royal 13"/Riata 14" SkyLake -U (UMA/DIS) Schematics

01

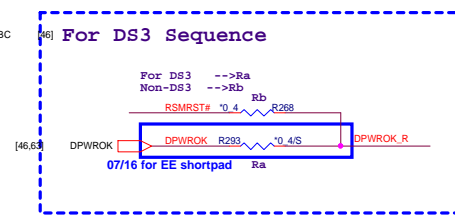
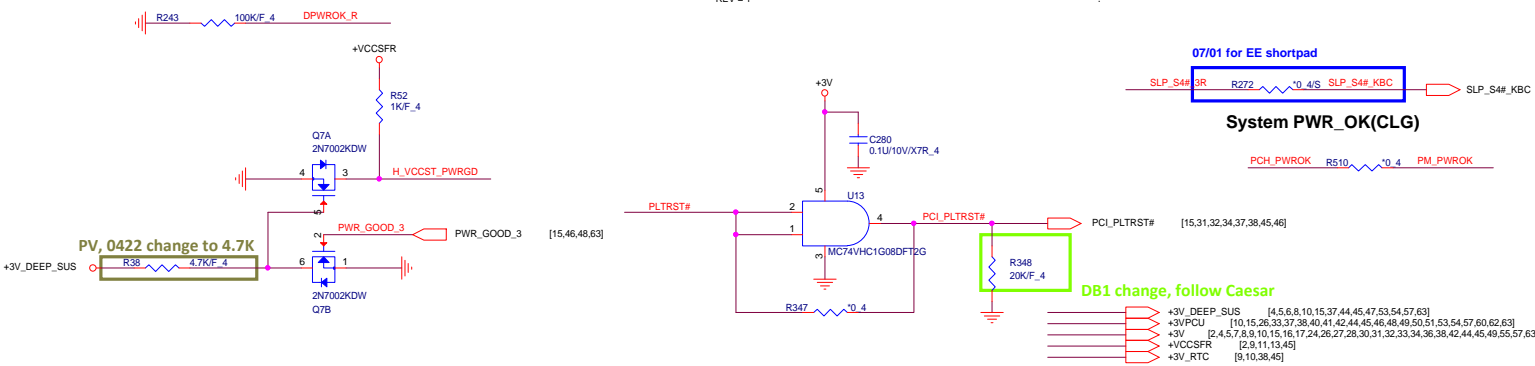
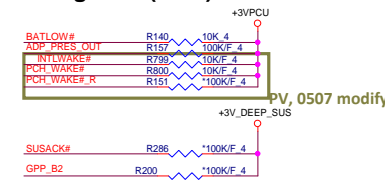
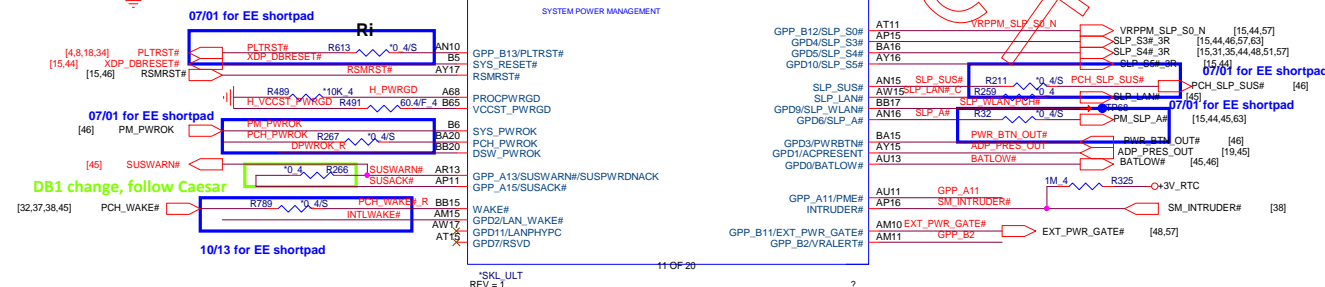
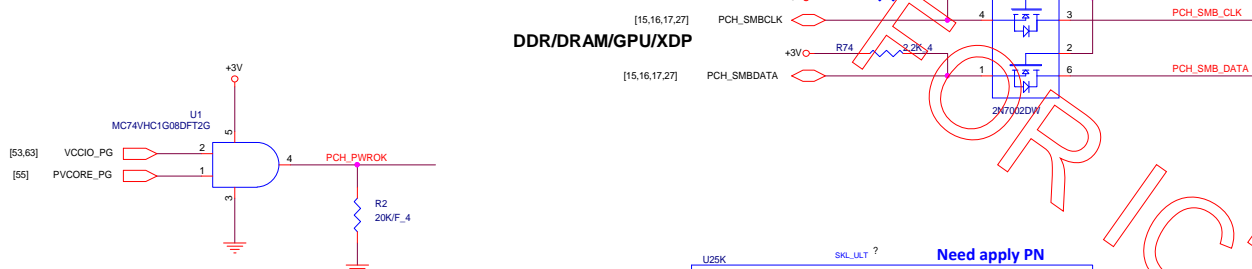


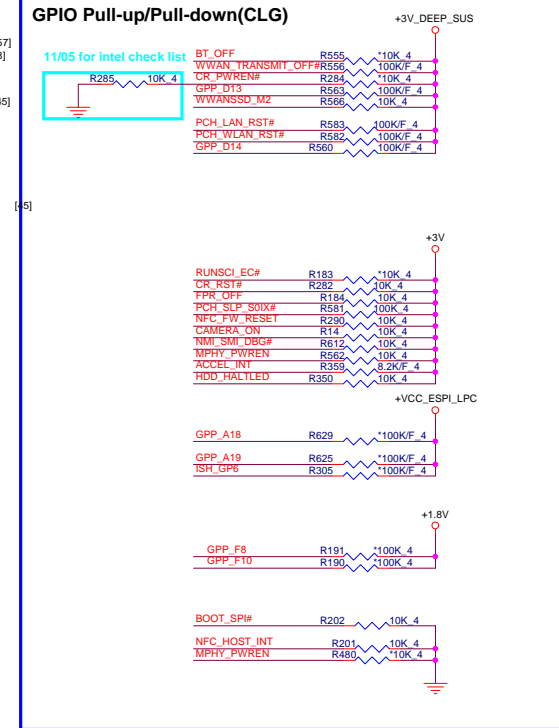
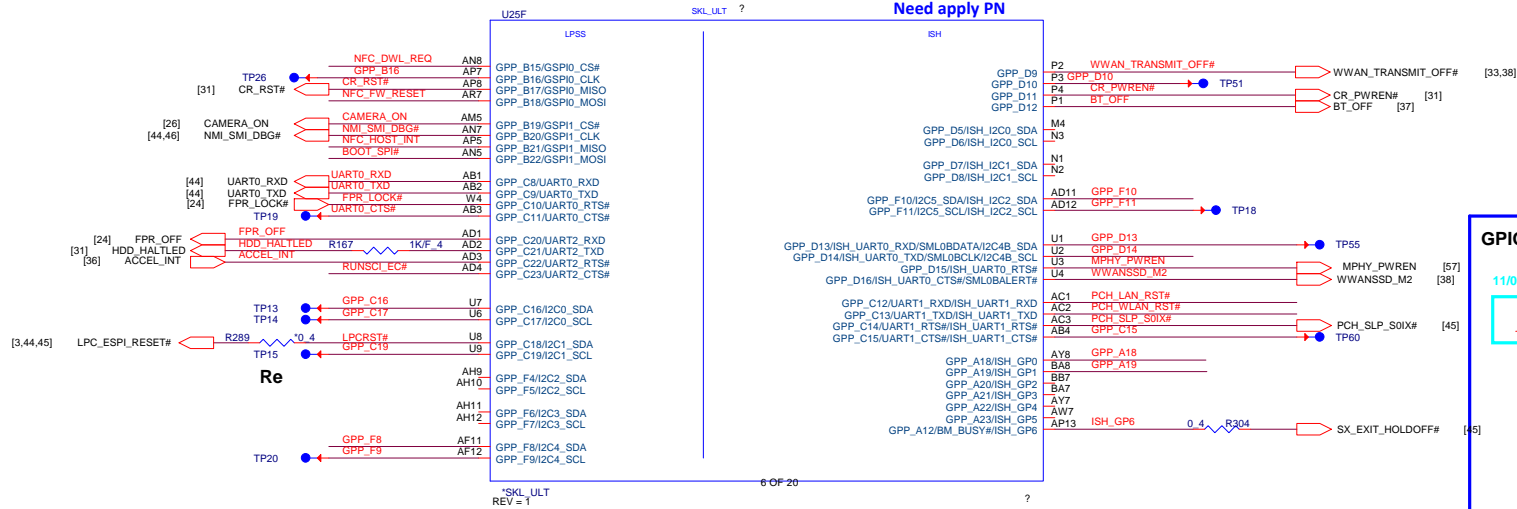




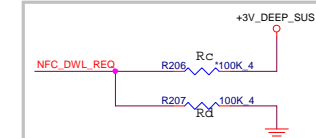
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R620	Ra 15Ω	15Ω
R621	Rb 15Ω	15Ω
R633	Rc 15Ω	15Ω
R634	Rd 15Ω	15Ω
R289	Re INSTAL	UNINSTAL
R636	Rf UNINSTAL	INSTAL
R61	Rg UNINSTAL	INSTAL
R67	Rh INSTAL	UNINSTAL
R613	Ri INSTAL	UNINSTAL
R183	Rj INSTAL	UNINSTAL

PCH Pull-high/low(CLG)



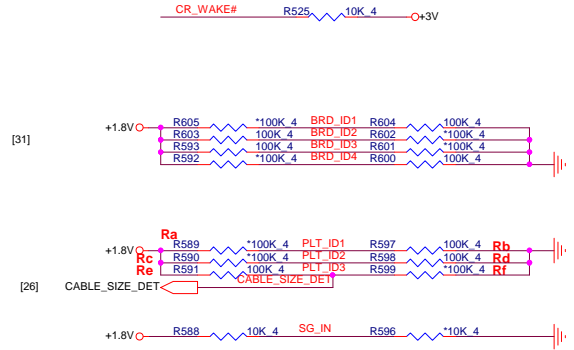
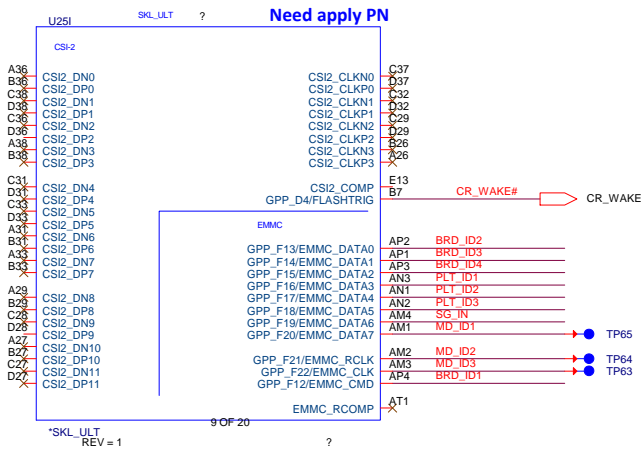


PV-R, 0701 for NFC_DWL_REQ WWAN & TS TABLE



WWAN & TS TABLE		
	WWAN MODE	TS MODE
R206	INSTAL	UNINSTAL
R207	UNINSTAL	INSTAL

	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2(DDR4)	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SIB	0	1	0	1	
SI2(DDR4)	0	1	1	0	
	0	1	1	1	
PV1	1	0	0	0	
PV-R	1	0	0	1	
PV2(DDR4)	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
MV2(DDR4)	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



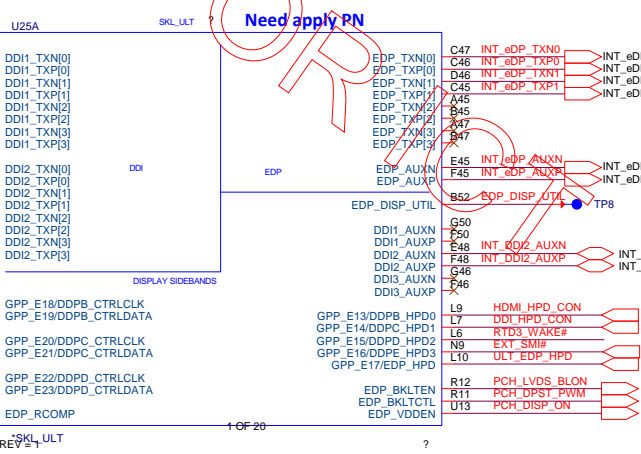
PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	0	15.6"
0	1	1	17.3"

SG_IN	SG_IN
R596	R588
UMA	DIS

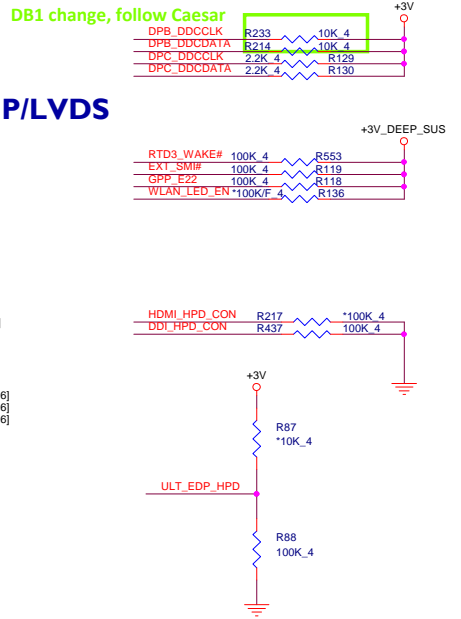
HDMI

VGA

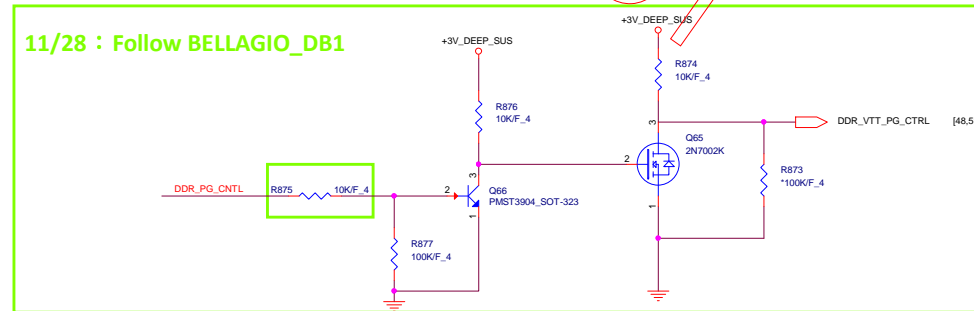
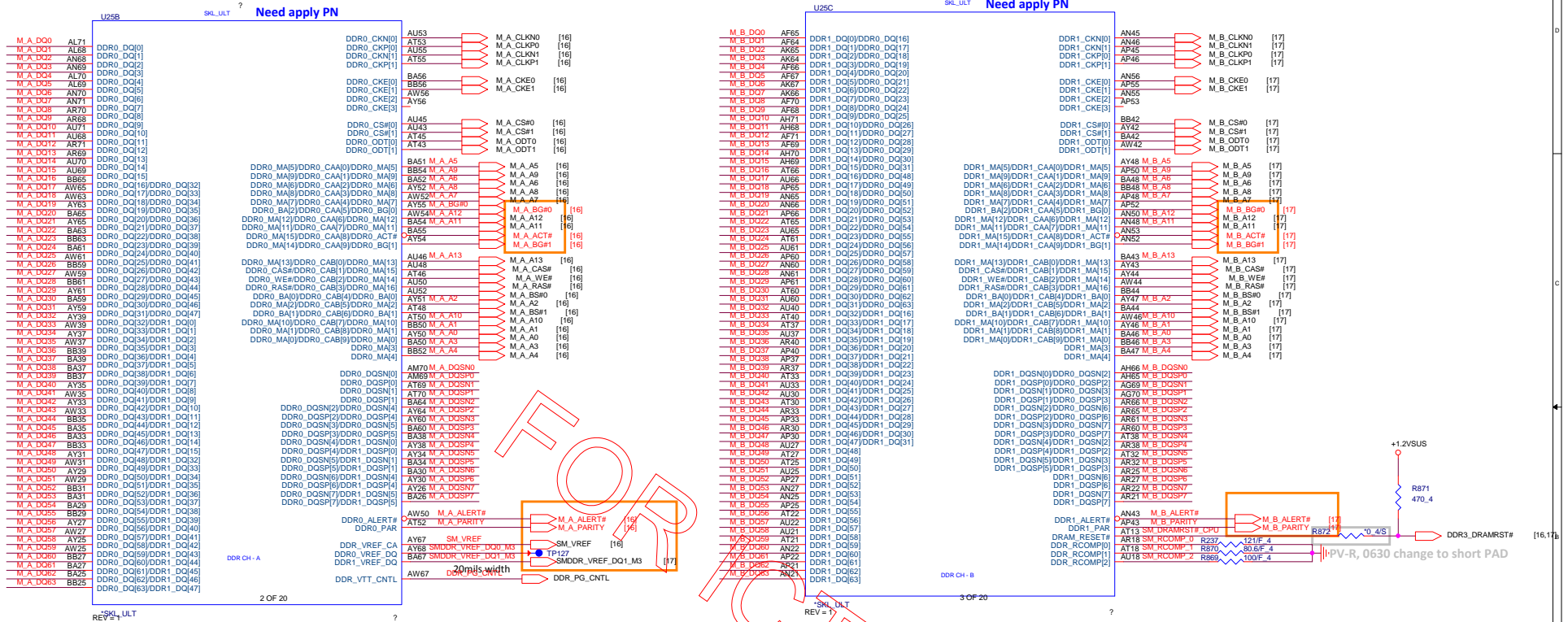
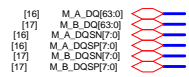
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



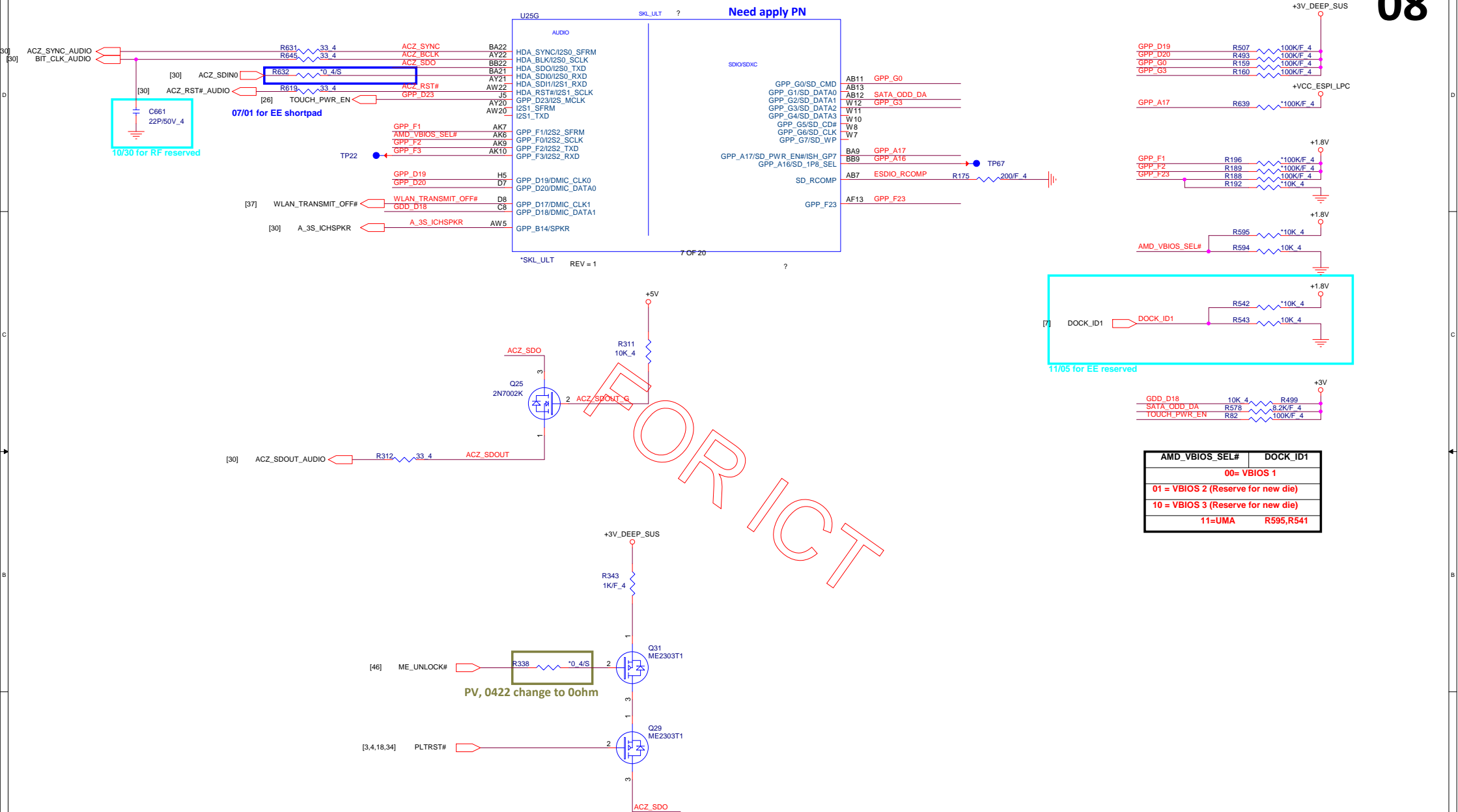
eDP/LVDS



SkyLake ULT Processor (DDR4)

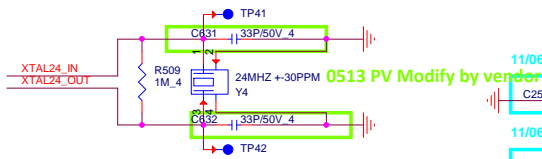
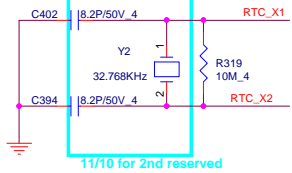






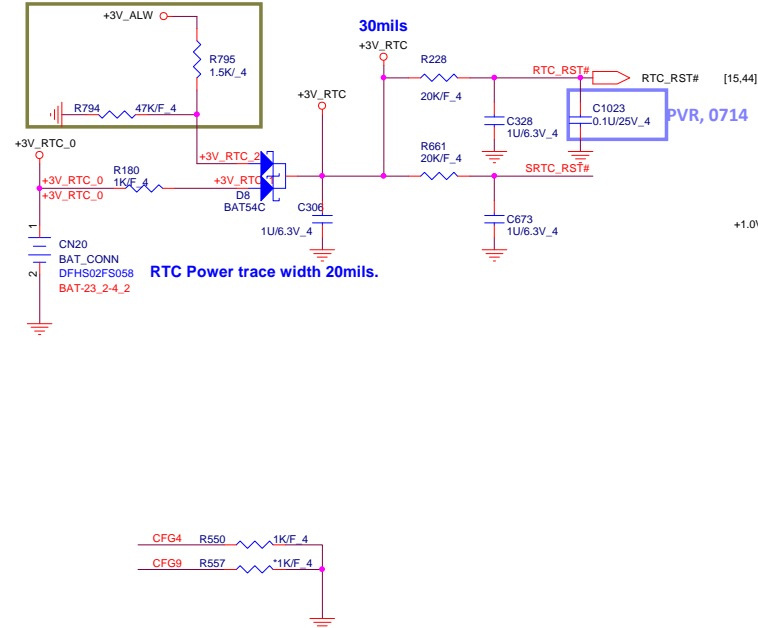
TBT

RTC Clock 32.768KHz



RTC Circuitry(RTC)

PV, 0413 add R795, R794 to prevent RTC power over +3.2V



+VCCSFR [2,3,11,13,45]
+1.0V_DEEP_SUS [10,15,52,53,54,57]
+3V [2,3,4,5,7,8,10,15,16,17,24,26,27,28,30,31,32,33,34,36,38,42,44,45,49,55,57,63]

Cardreader

LAN

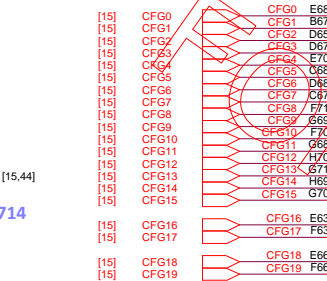
WLAN

dGPU

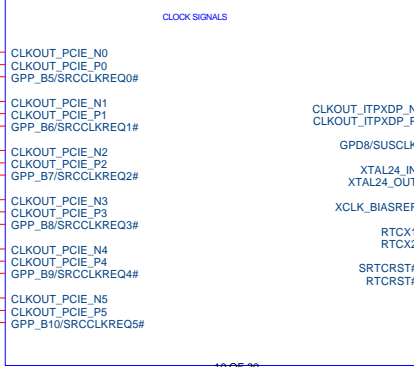
11/06 for RF reserved

11/06 for RF reserved

CFG0-19 need Reserve TP

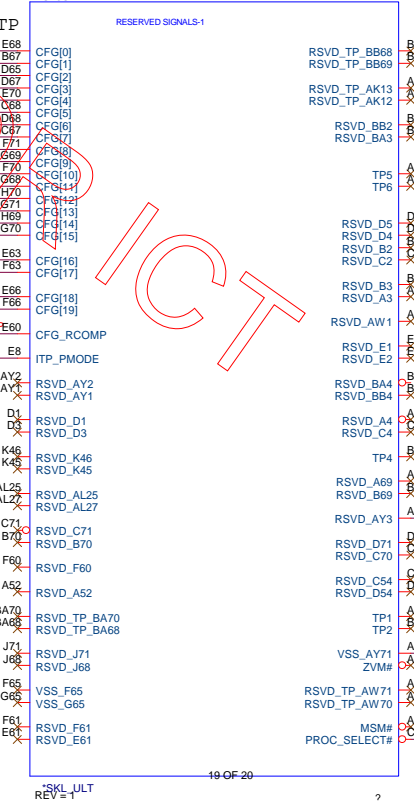


Need apply PN



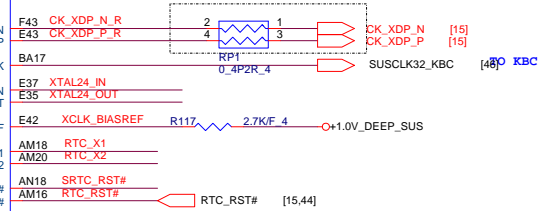
*SKL_ULT REV=1

Need apply PN

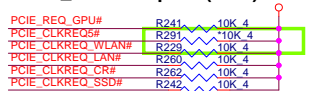


*SKL_ULT REV=1

RP1 install for XDP

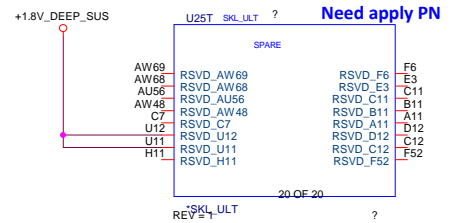


CLK_REQ/Strap Pin(CLG)



0421 PV Modify

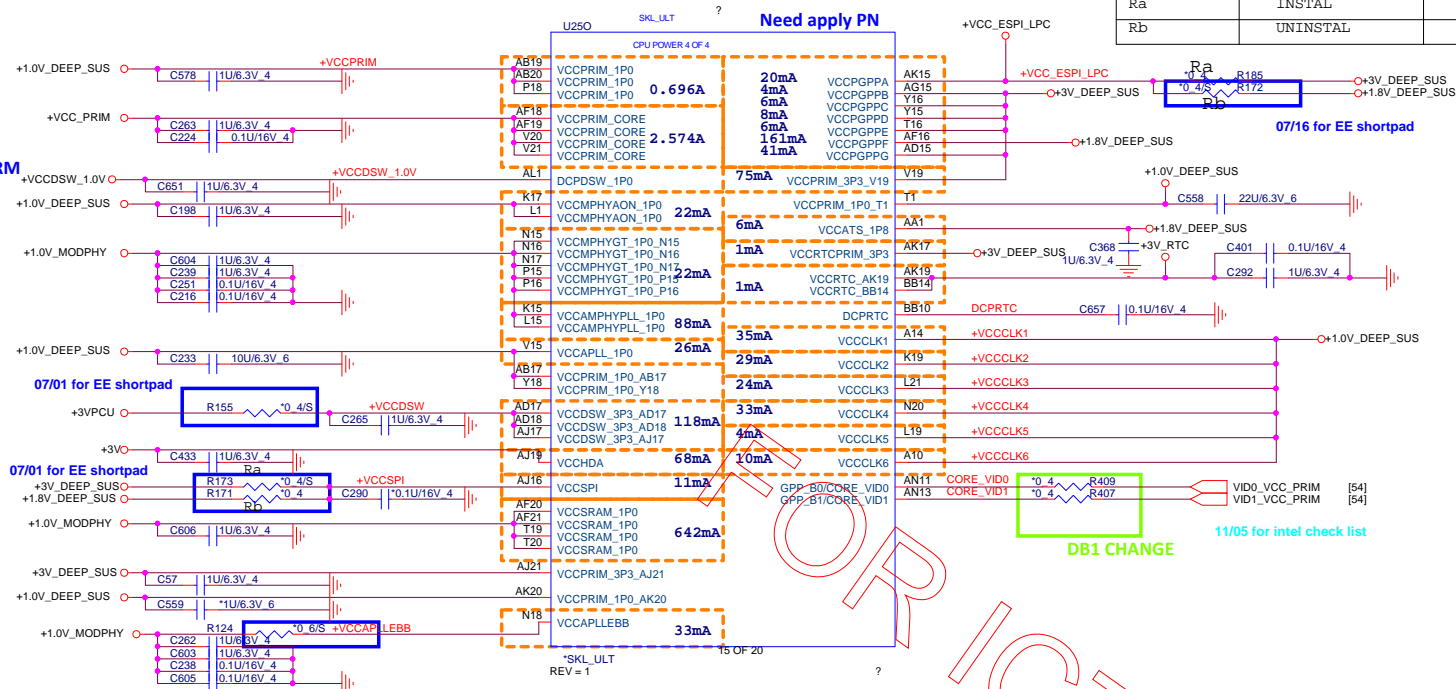
Need apply PN



PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 - SKYLAKE (CLK/RSV/RTC)	1A
Date: Monday, November 30, 2015	Sheet	9 of 65

PCH Internal VRM

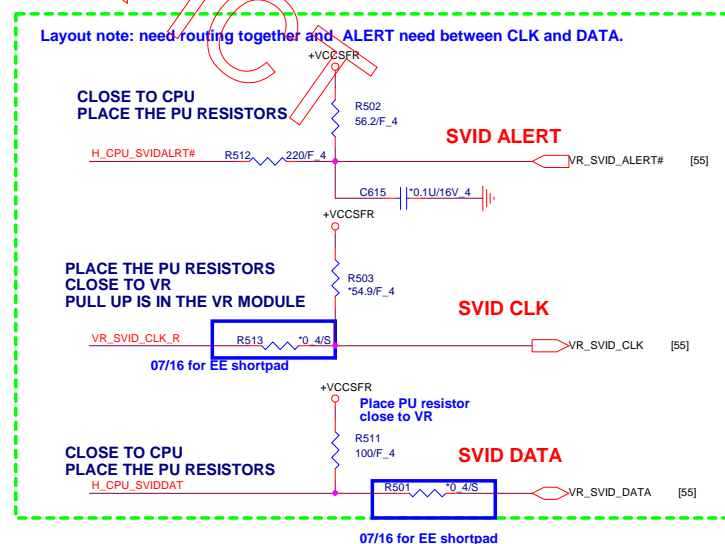
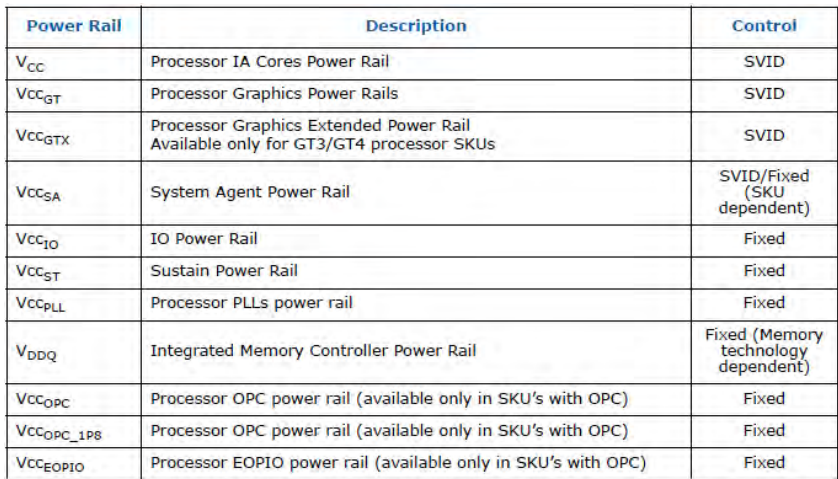


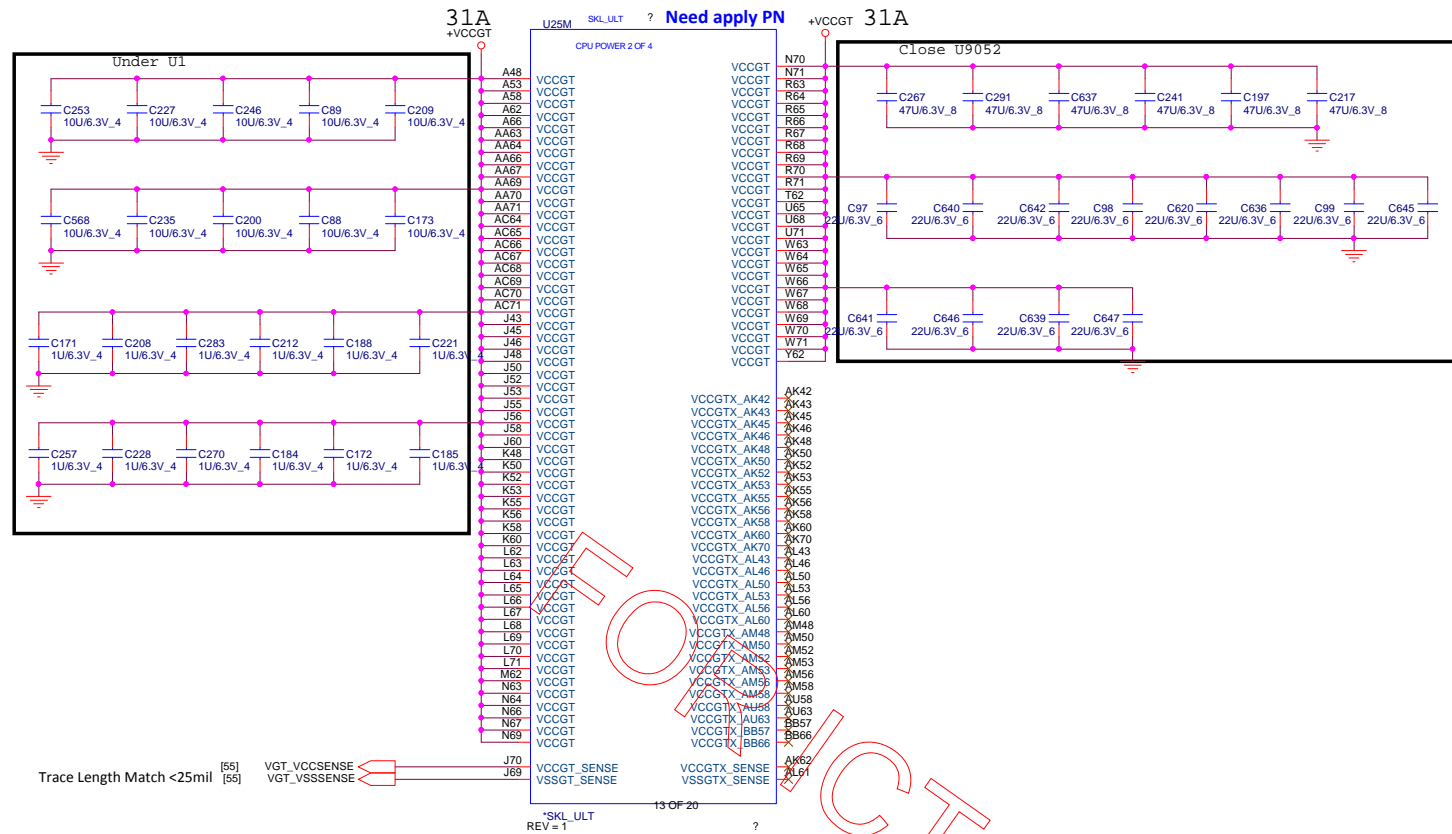
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	INSTAL	UNINSTAL
Rb	UNINSTAL	INSTAL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	INSTAL	UNINSTAL
Rb	UNINSTAL	INSTAL

+3V_DEEP_SUS [3,4,5,6,8,15,37,44,45,47,53,54,57,63]
 +3VPCU [3,15,26,33,37,38,40,41,42,44,45,46,48,49,50,51,53,54,57,60,62,63]
 +1.0V_DEEP_SUS [9,15,52,53,54,57]
 +VCCPRIM [25,54]
 +3V [2,3,4,5,7,8,9,15,16,17,24,26,27,28,30,31,32,33,34,36,38,42,44,45,49,55,57,63]
 +1.8V_DEEP_SUS [9,45,47,52,63]

	PROJECT:400 Series		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number 10 - SKYLAKE (PCH POWER)	
Date: Monday, November 30, 2015		Sheet 10 of 65	

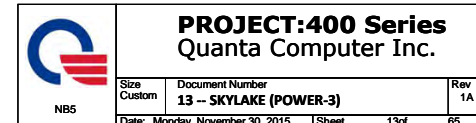




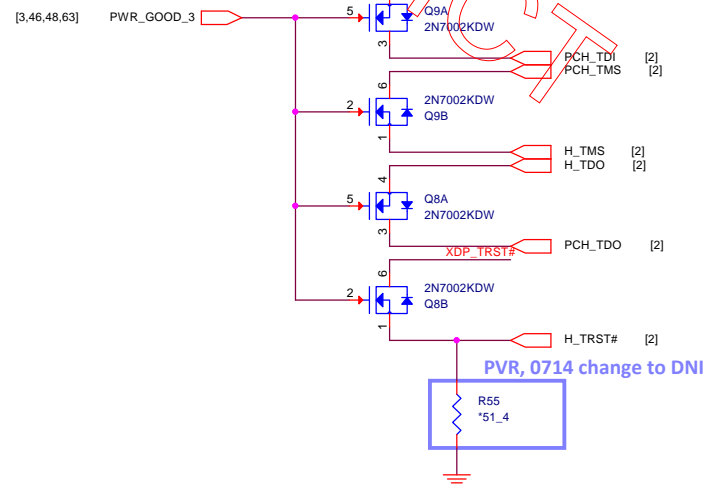
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

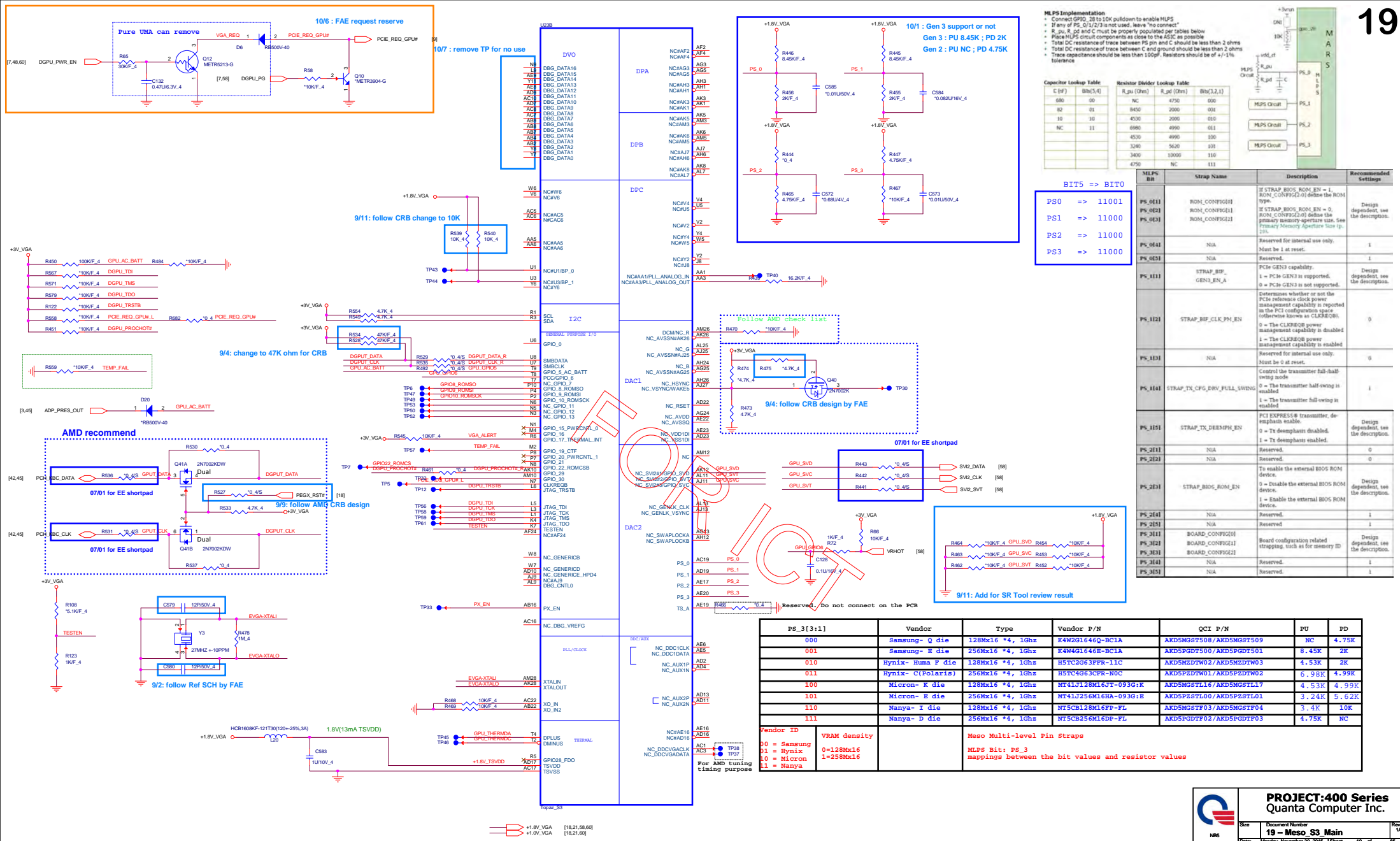


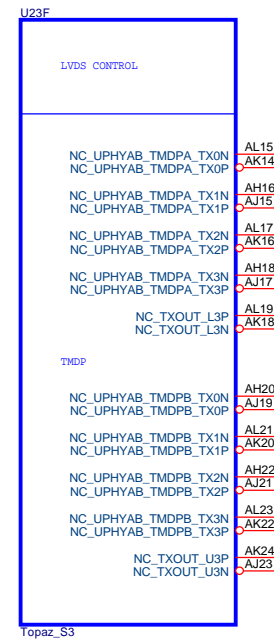
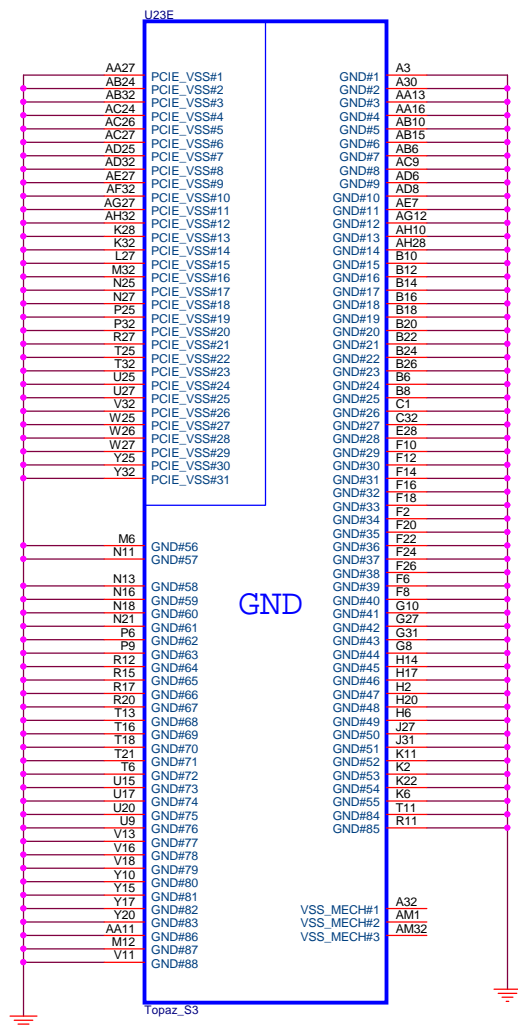












CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

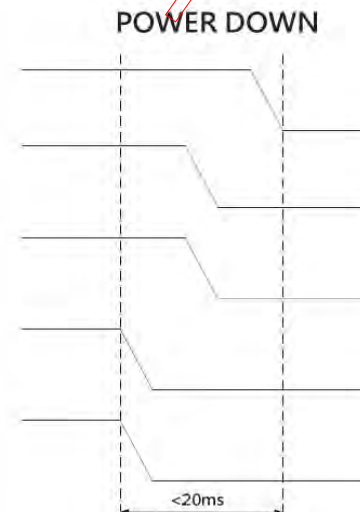
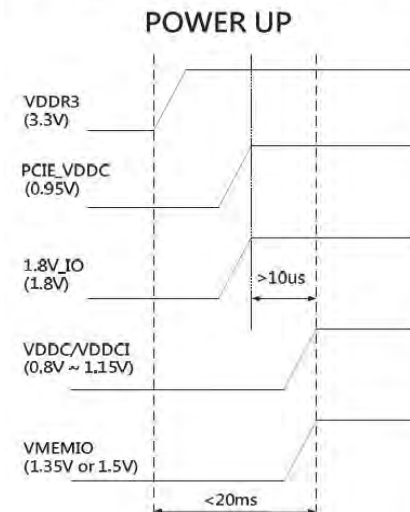
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

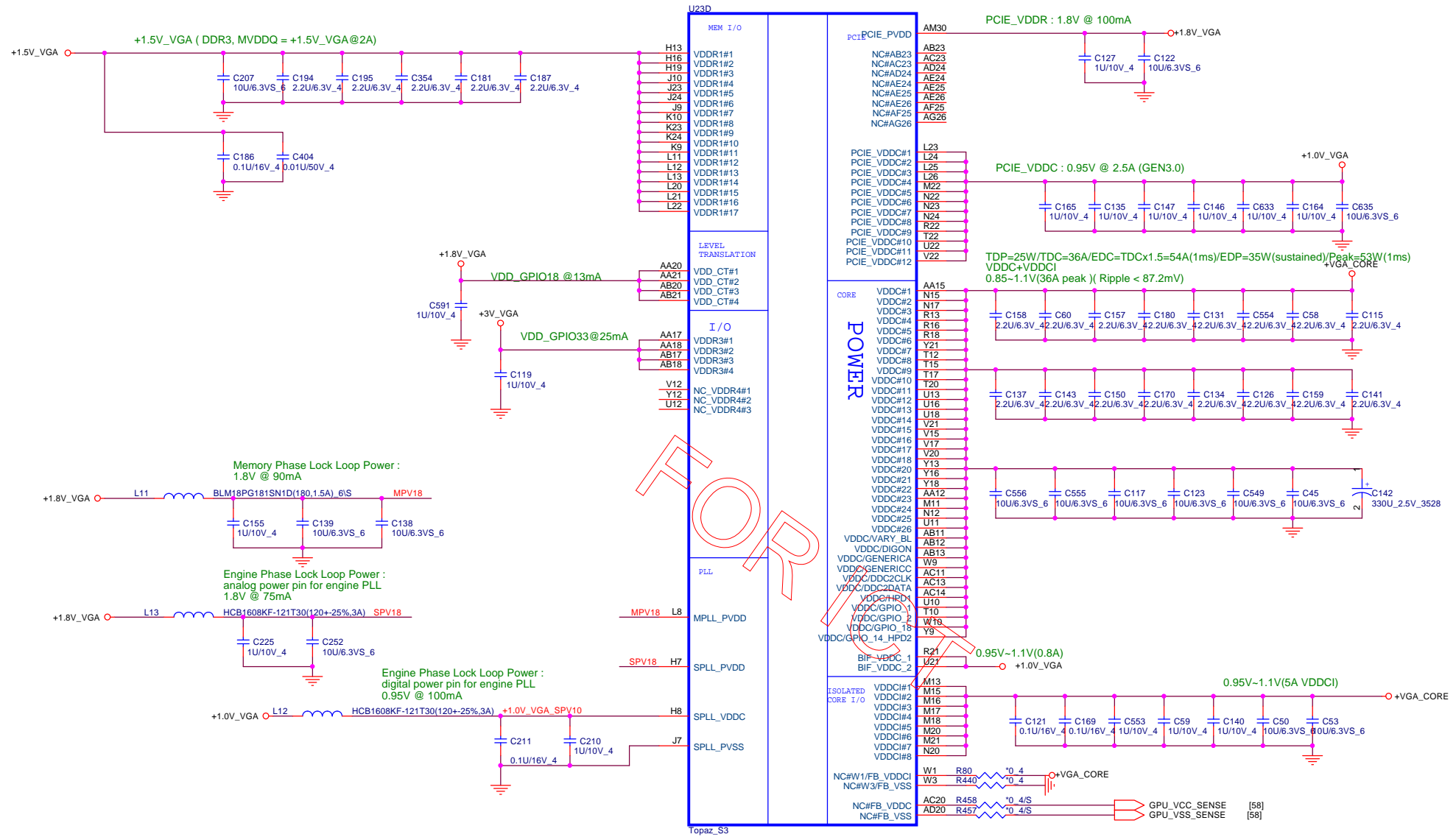
POWER UP / POWER DOWN SEQUENCE

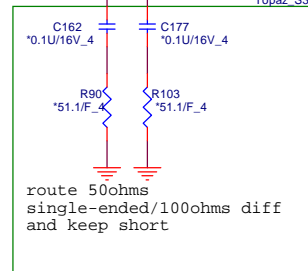
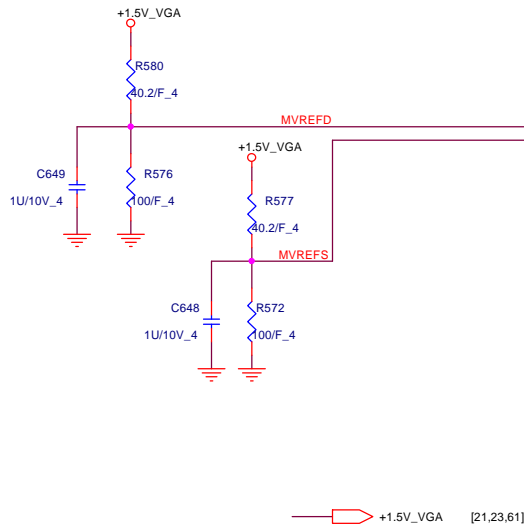
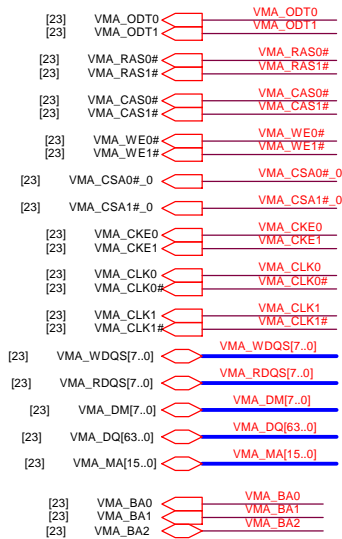


PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
	20 - Meso_S3_GND/LVDS/Strap	1A
Date:	Monday, November 30, 2015	Sheet 20 of 65

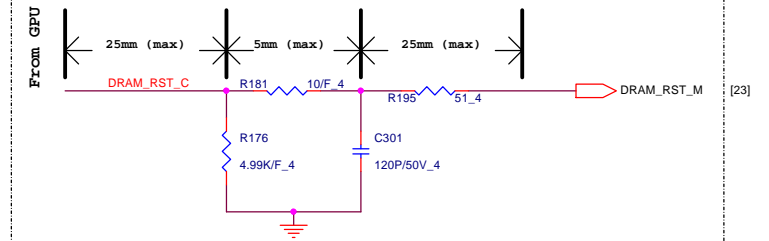
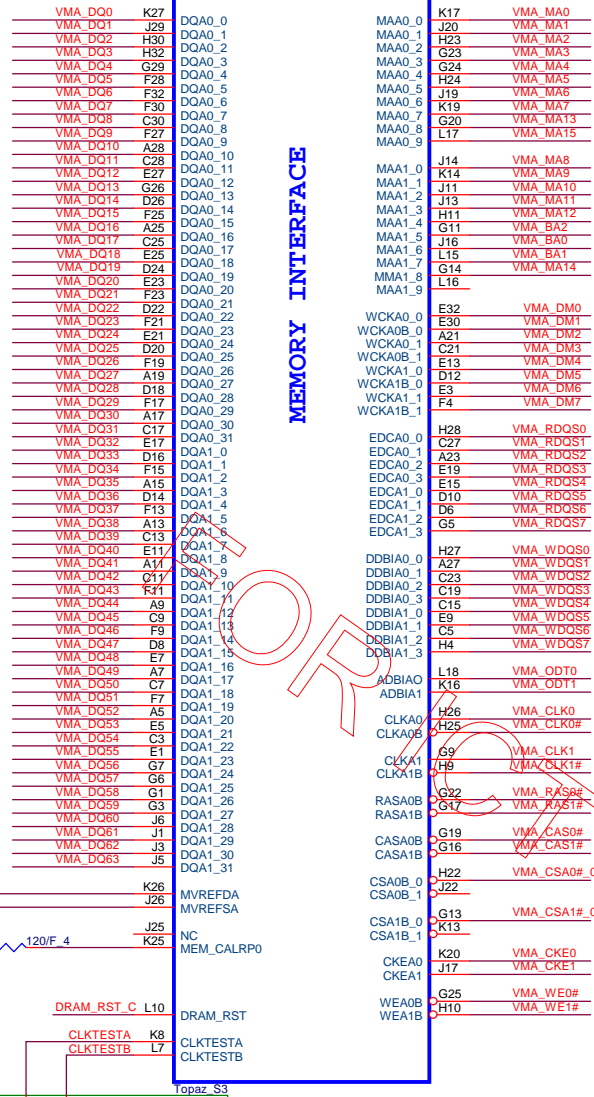
NB5





U23C

MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.



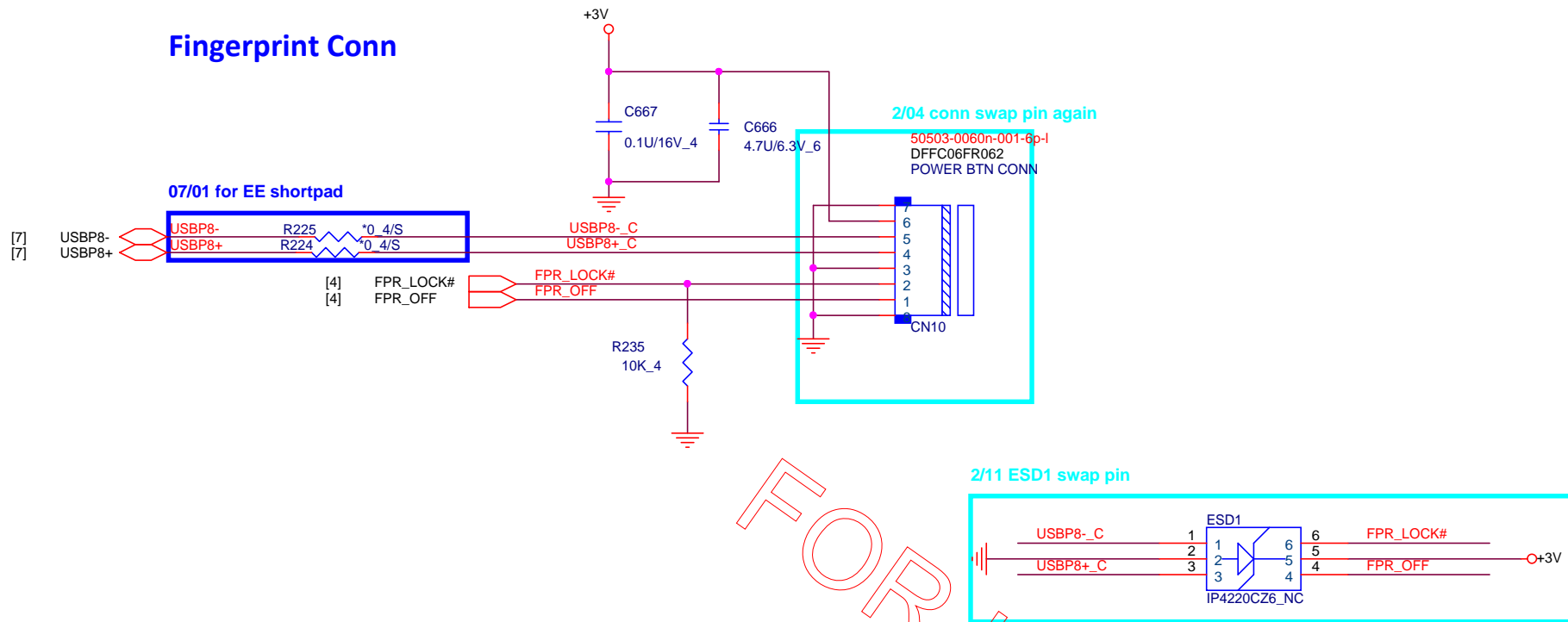
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
	22 - Meso_S3_MEM_Interface	1A
Date:	Monday, November 30, 2015	Sheet 22 of 65


NB5



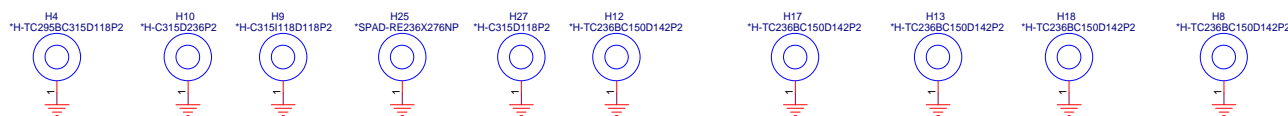
Fingerprint Conn



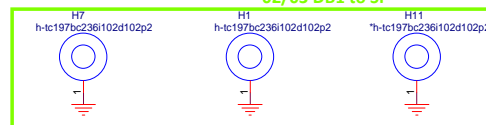
FOR ICT

 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 24 -- FPR	Rev 1A
	Date: Monday, November 30, 2015	Sheet 24 of 65	

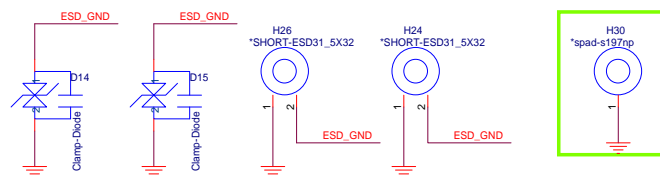
Hole



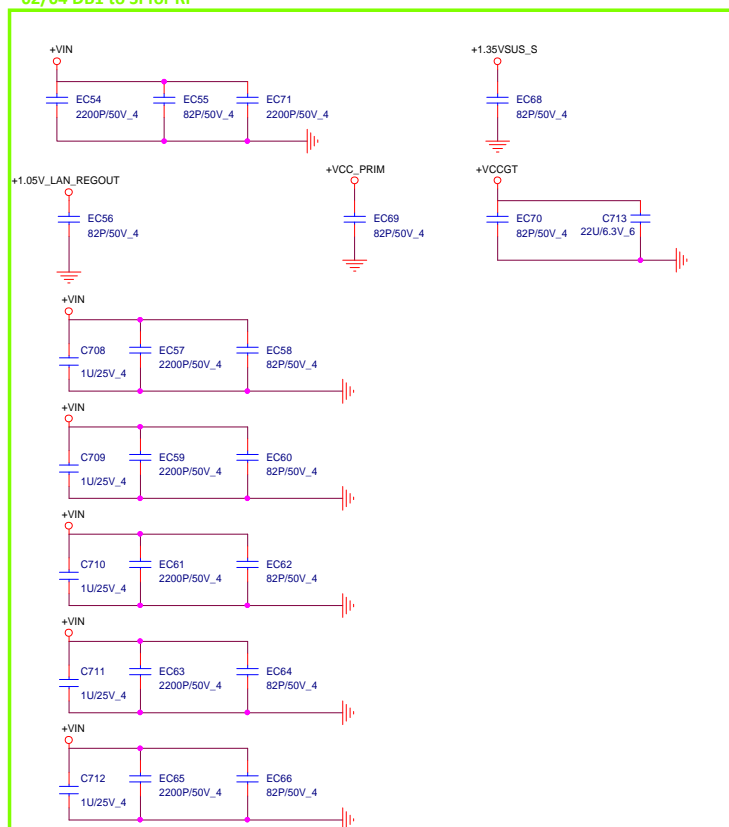
02/03 DB1 to SI



02/11 DB1 to SI



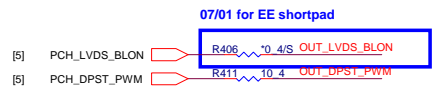
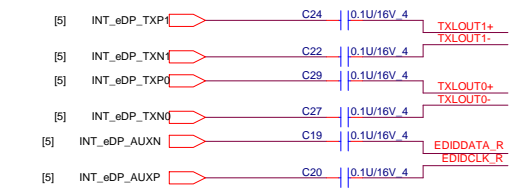
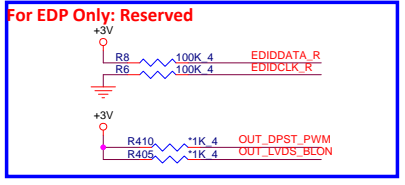
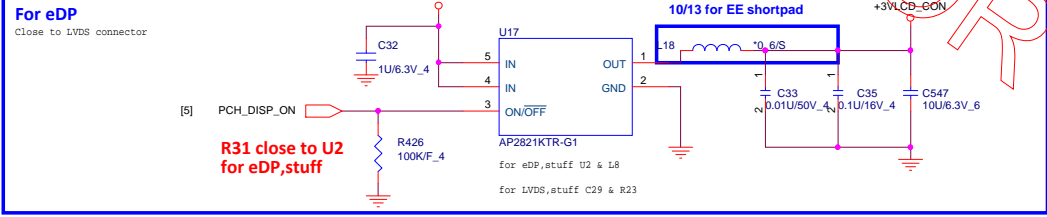
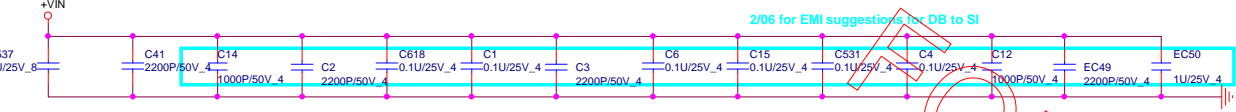
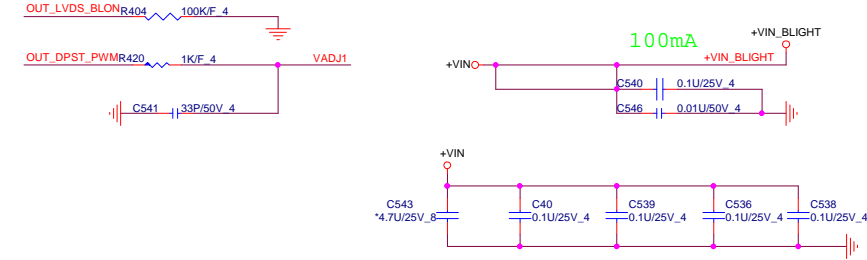
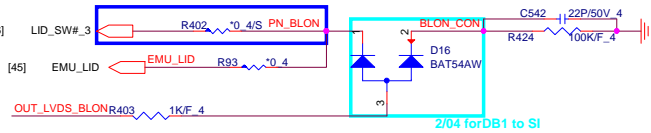
02/04 DB1 to SI for RF



FOR ICT

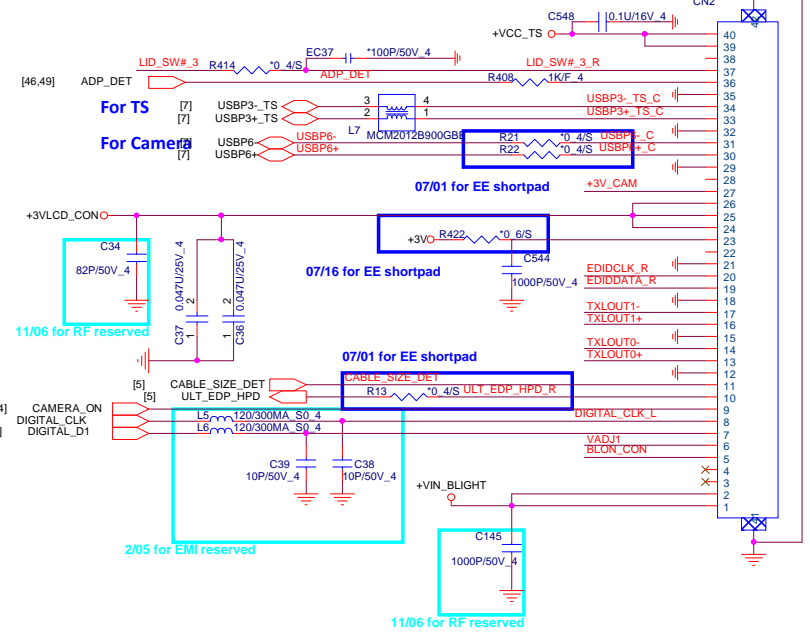
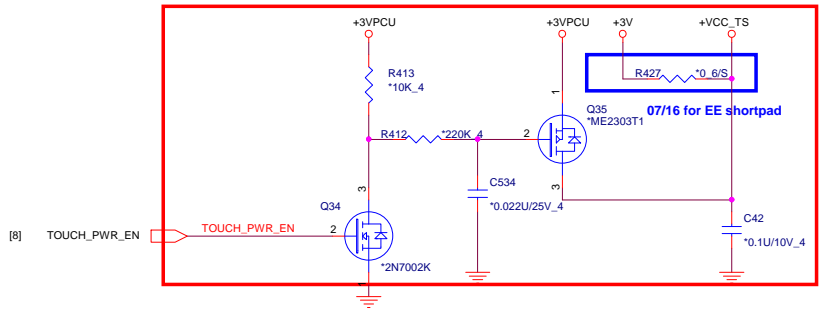
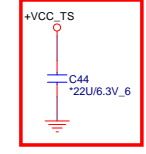
LID Switch

07/01 for EE shortpad




LVDS Conn.

26



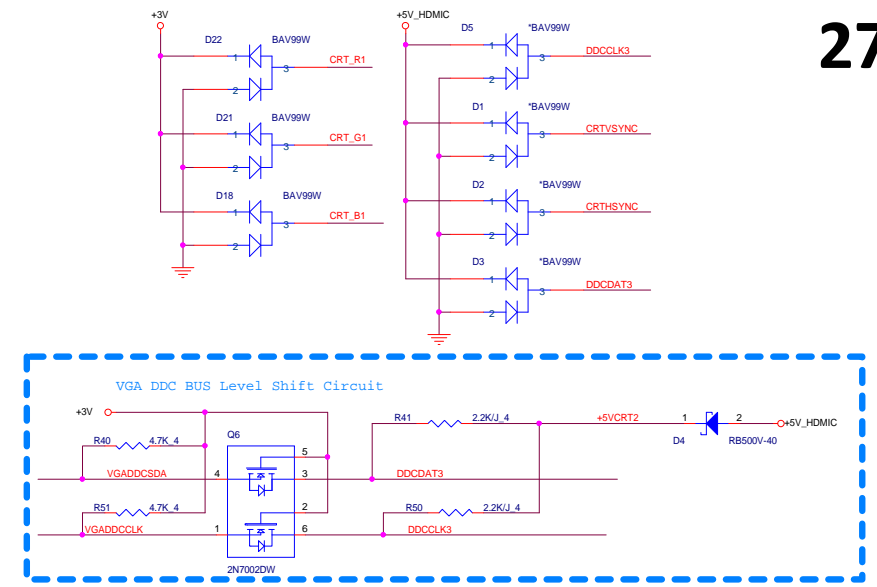
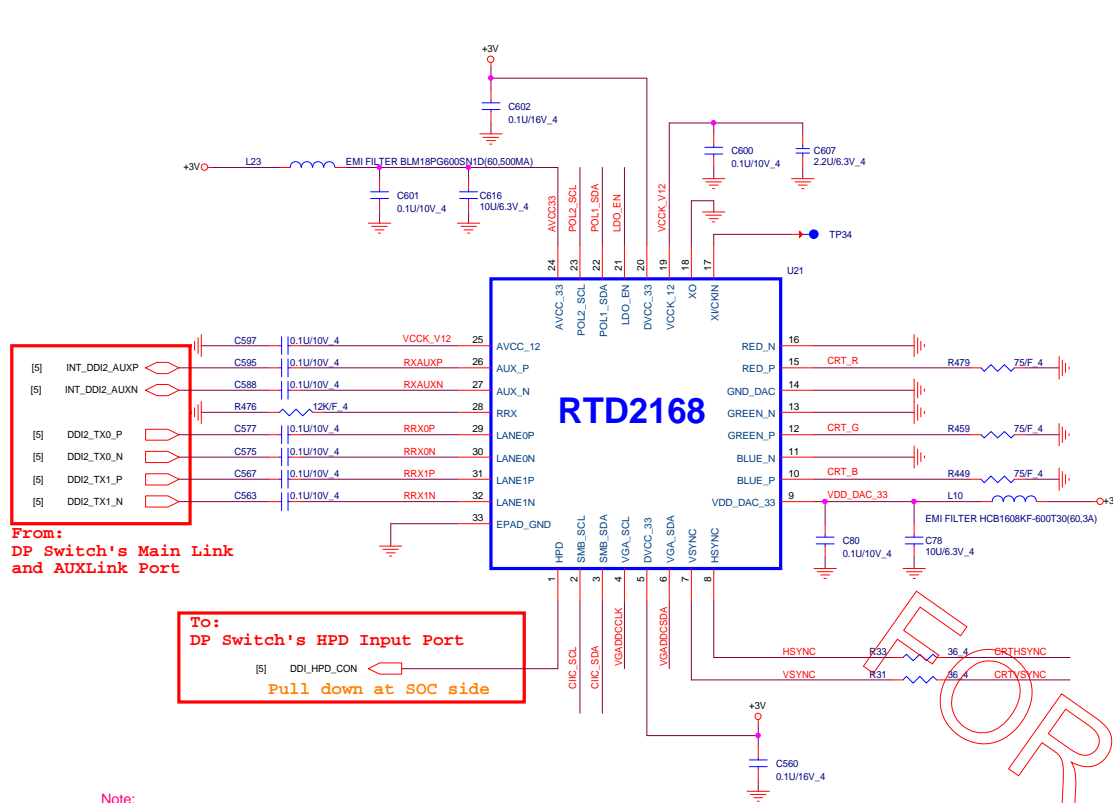
[2,3,4,5,7,8,9,10,15,16,17,24,27,28,30,31,32,33,34,36,38,42,44,45,49,55,57,63]
[8,29,30,31,40,42,43,52,57,63]
[25,44,49,50,51,52,53,54,55,56,57,59,61]

+3V
+5V
+VIN

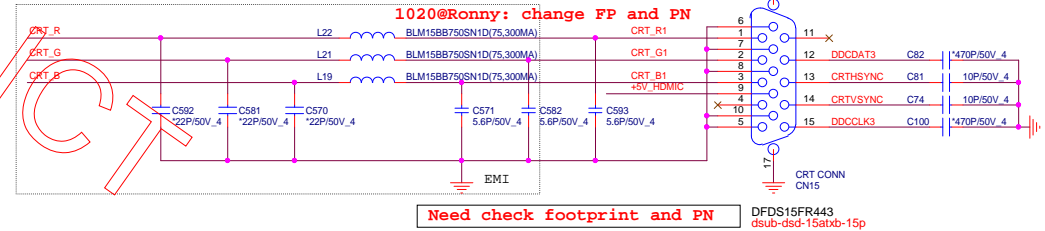


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Size Custom	Document Number 26 - LCD CONN/LID/CAM/D-MIC	Rev 1A
Date: Monday, November 30, 2015		Sheet 26 of 65

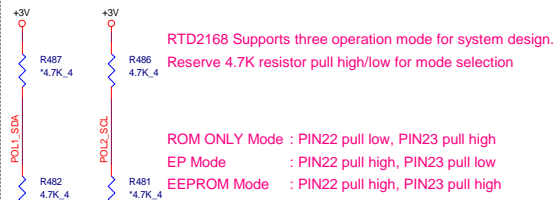


1103@RNY:
need change L11~L13 to 0402 size PN and value



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EPPROM MODE



EEPROM MODE

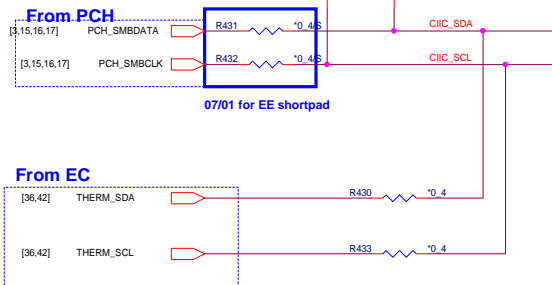
In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following conditions.

- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

CIIC_SCL, CIIC_SDA Connection

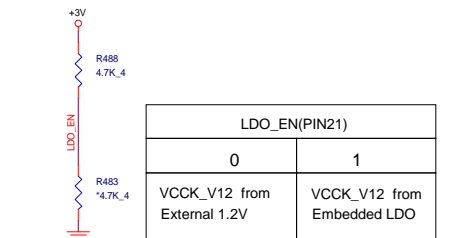
EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



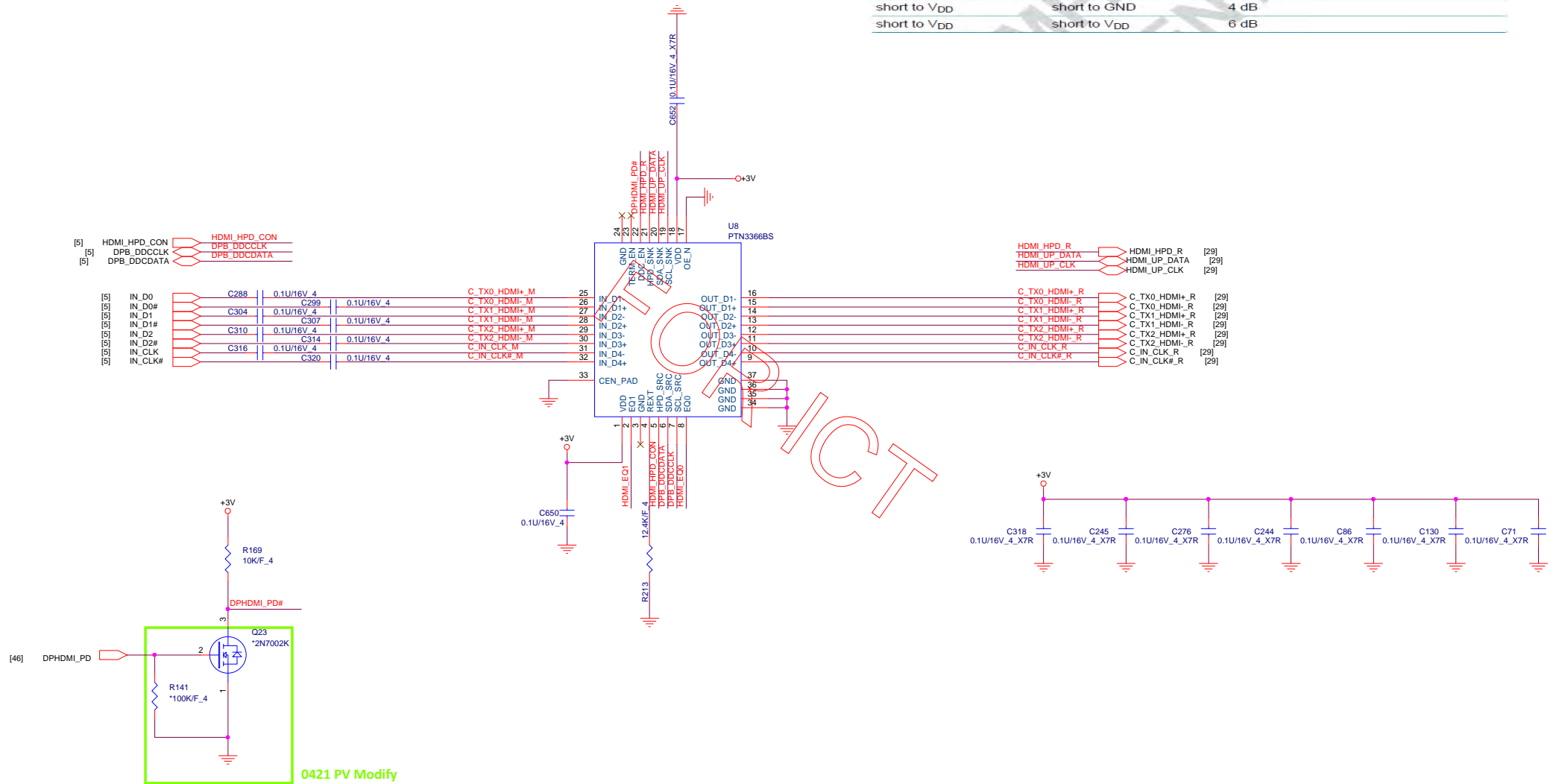
Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO



PROJECT : S Class-AMD
Quanta Computer Inc.

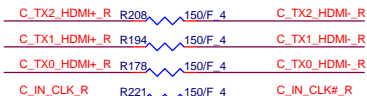
Size Custom Document Number DP to VGA
Date: Monday, November 30, 2015 Sheet 27 of 65



Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V _{DD}	2 dB
short to V _{DD}	short to GND	4 dB
short to V _{DD}	short to V _{DD}	6 dB

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

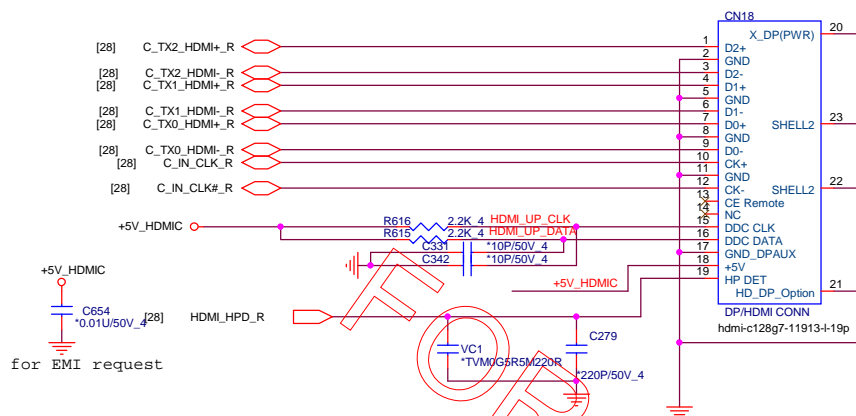
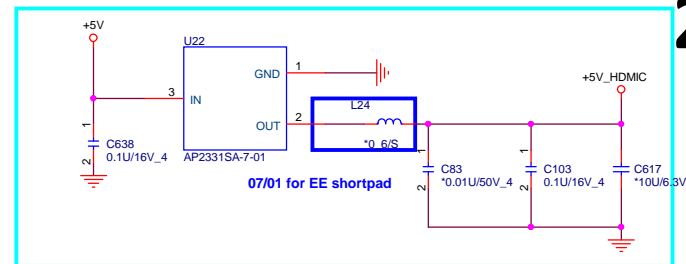
EMI Solution



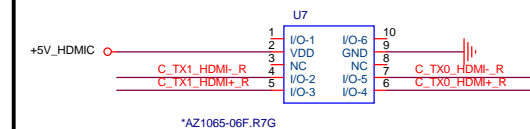
HDMI SMBus Isolation



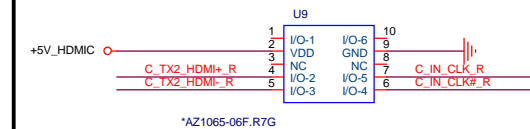
11/06 for change new SW

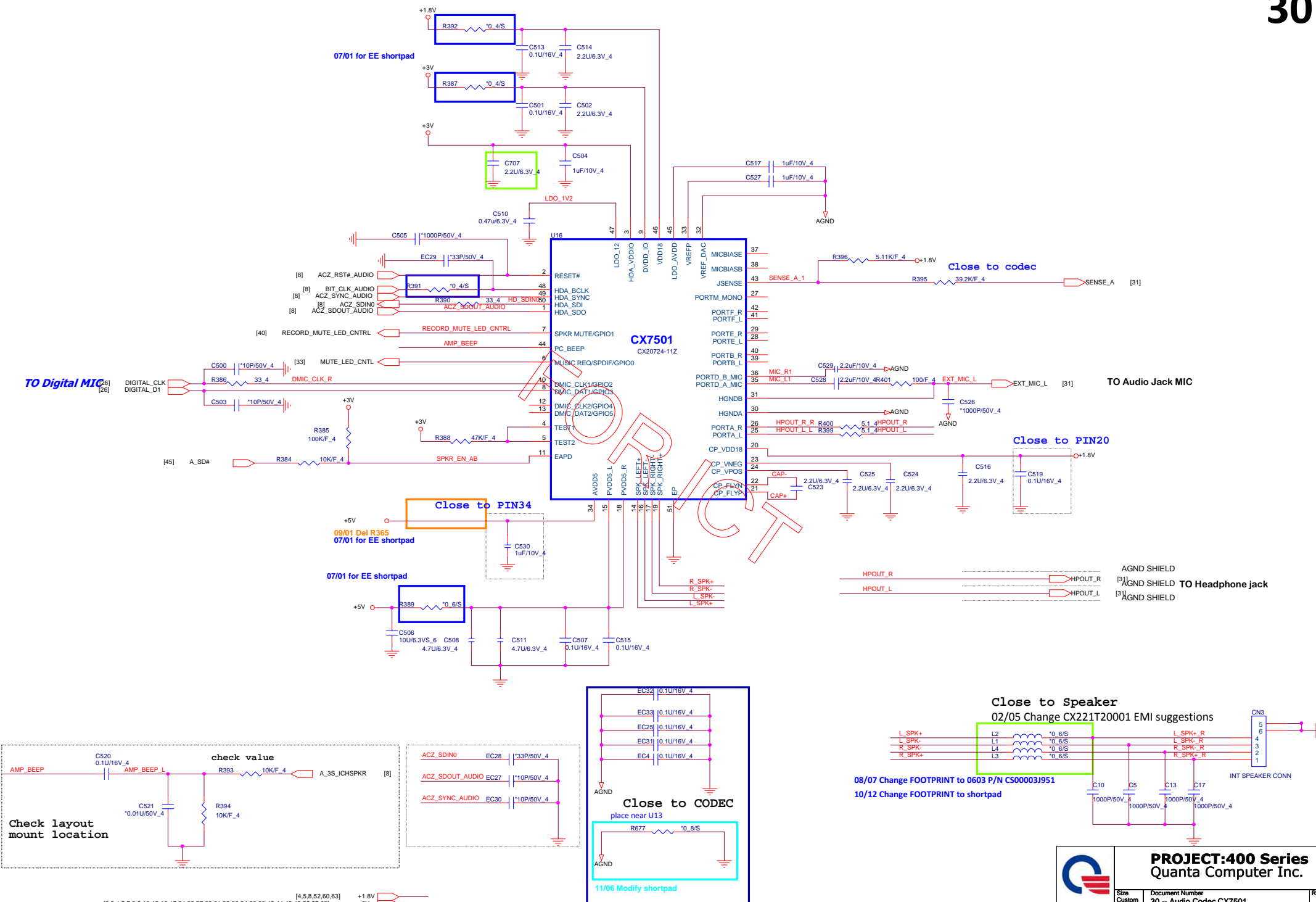


ESD chip, reserve

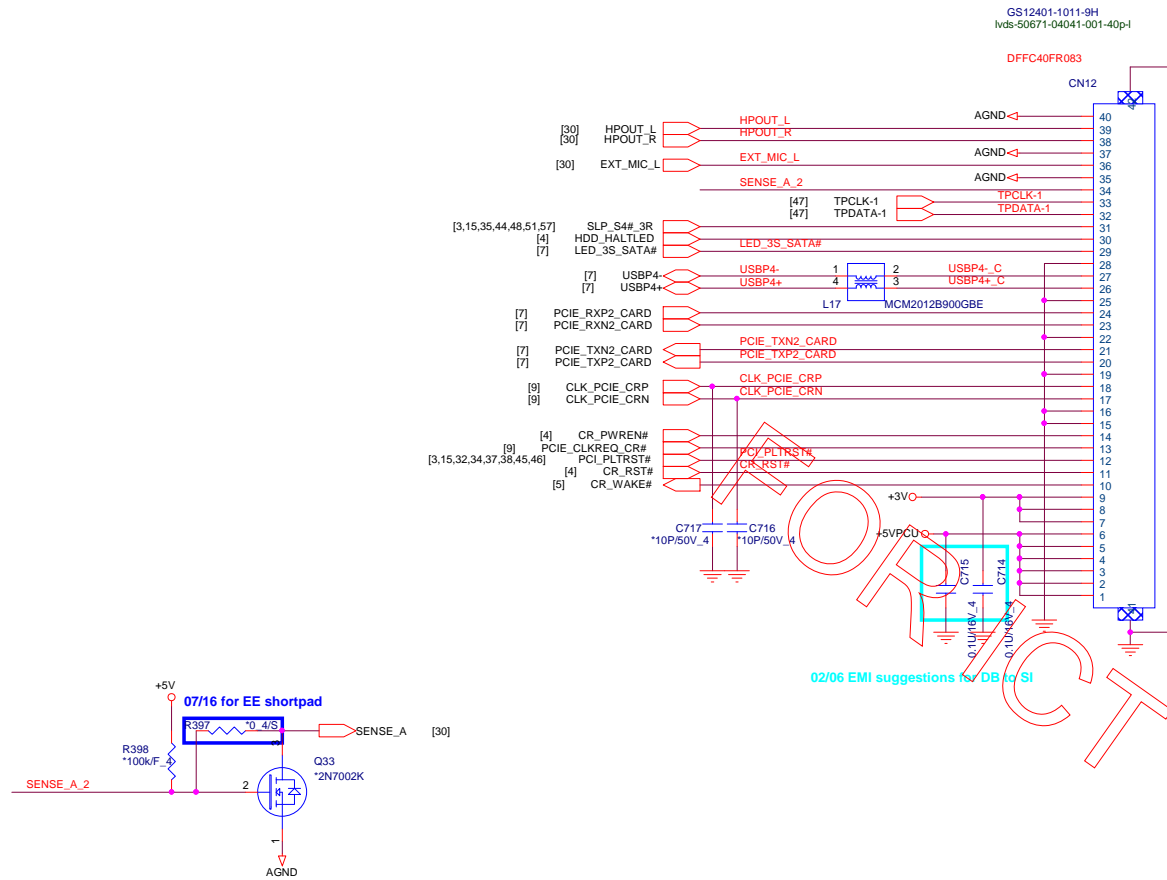



ESD chip, reserve

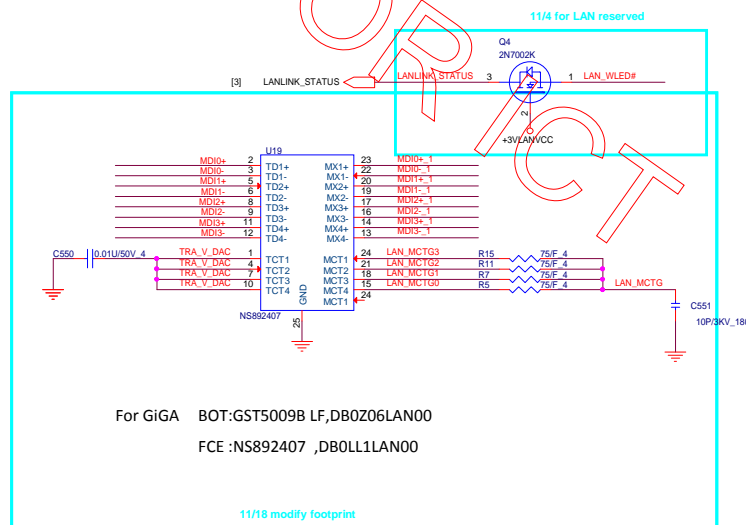
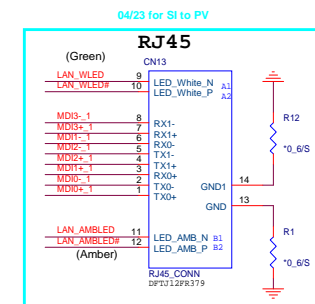
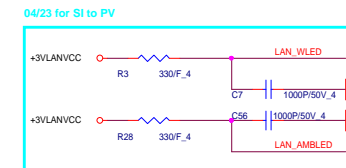
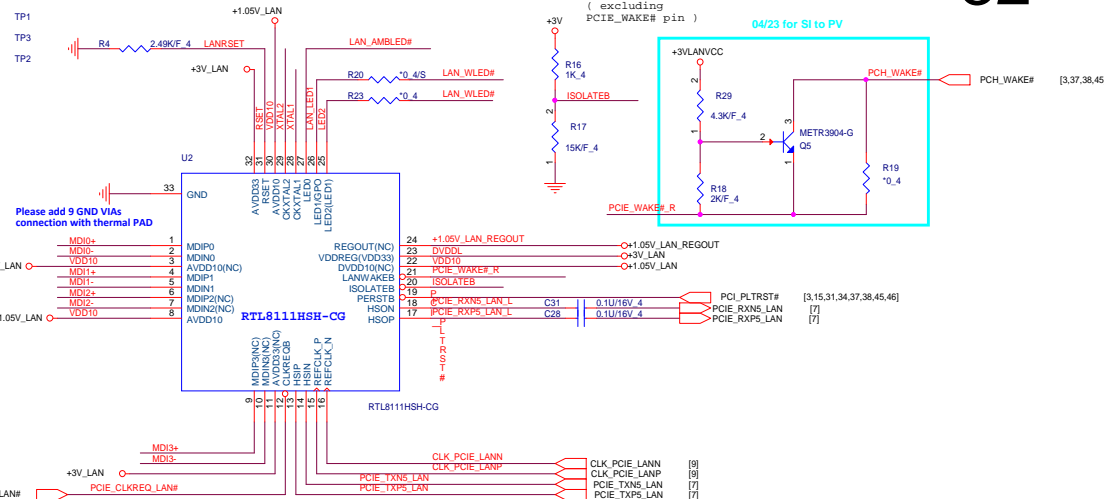
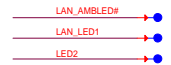




USB/Card Reader/Headphone_Mic Combo Jack Daughter Board Connector



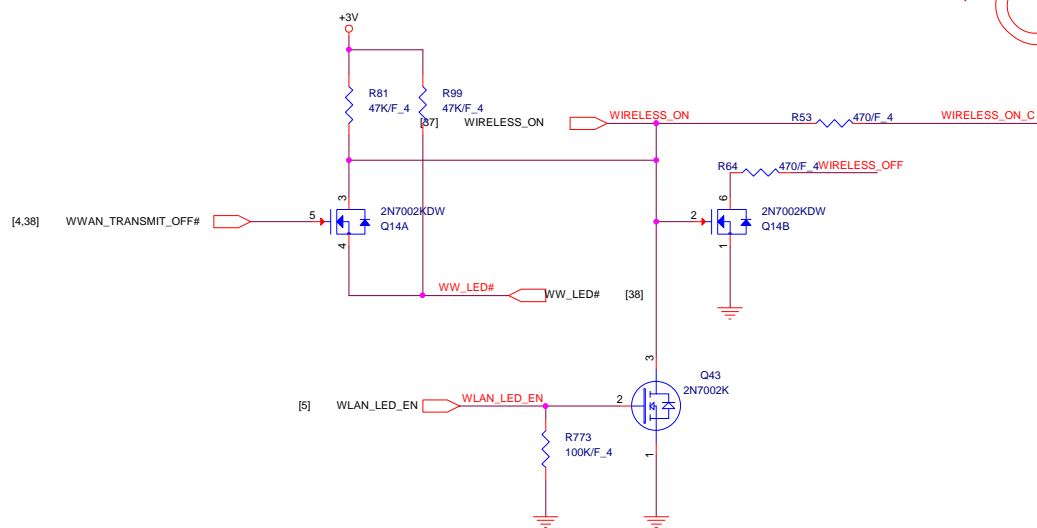
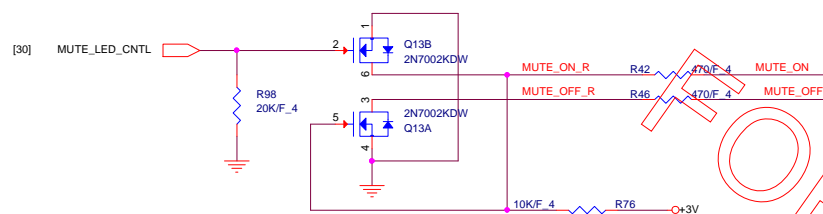
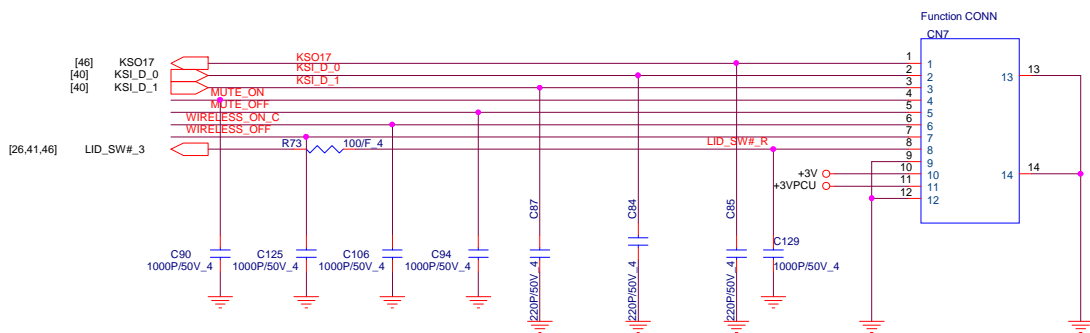
 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 31 -- DAUGHTER BOARD CONN.	Rev 1A
Date: Monday, November 30, 2015 Sheet 31 of 65			

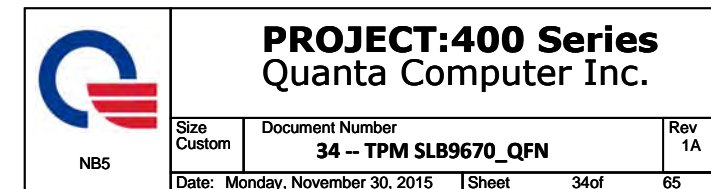


For GiGA BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,42,44,45,49,55,57,63]

[57] +3V
+3V1 ANVCC

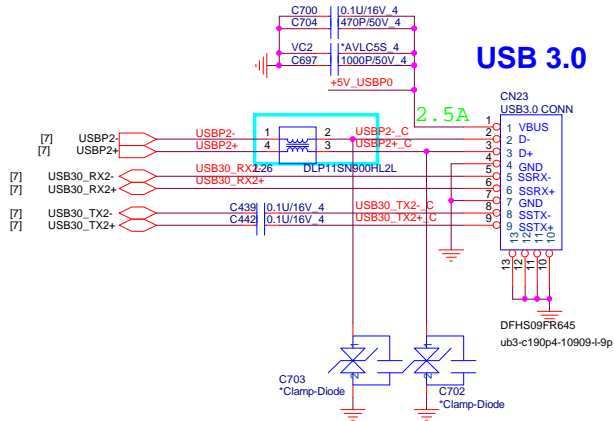
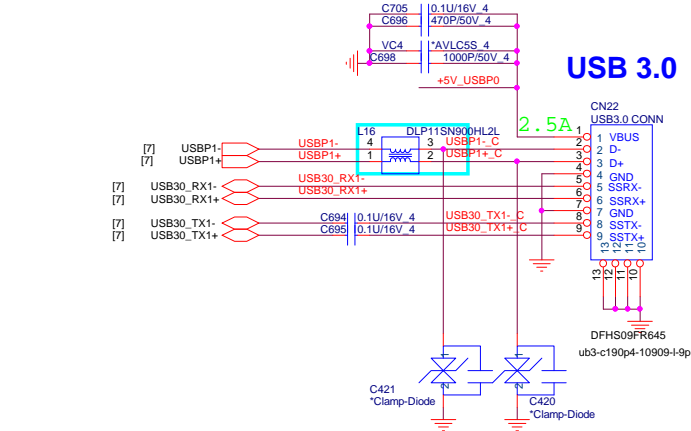




USB 2.0/3.0 Combo

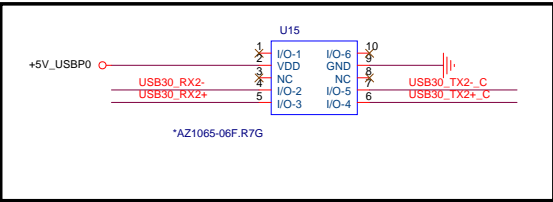
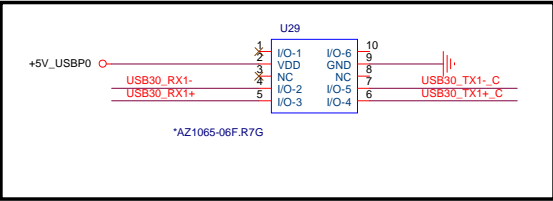
USB 3.0

USB 3.0



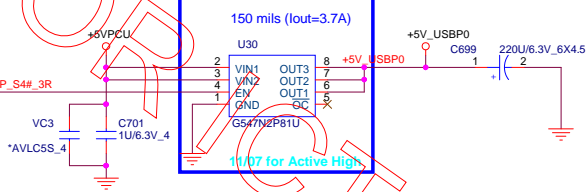
ESD chip, reserve

ESD chip, reserve



[3,15,31,44,48,51,57]

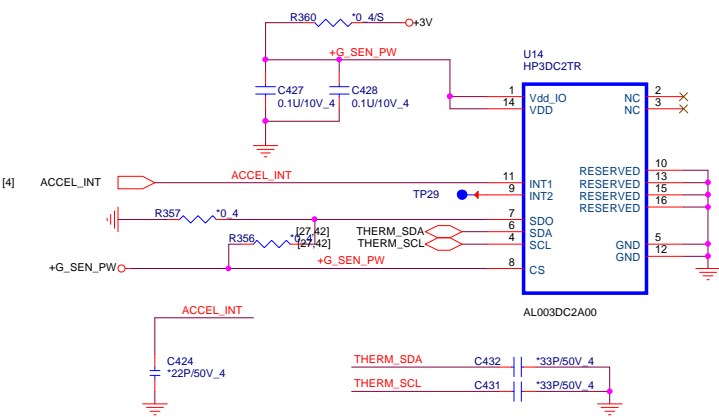
SLP_S4#_3R



[31,49,50,51,52,55,56,57,58,60,61,63]
[3,10,15,26,33,37,38,40,41,42,44,45,46,48,49,50,51,53,54,57,60,62,63]

+5VPCU
+3VPCU

Accelerometer Sensor



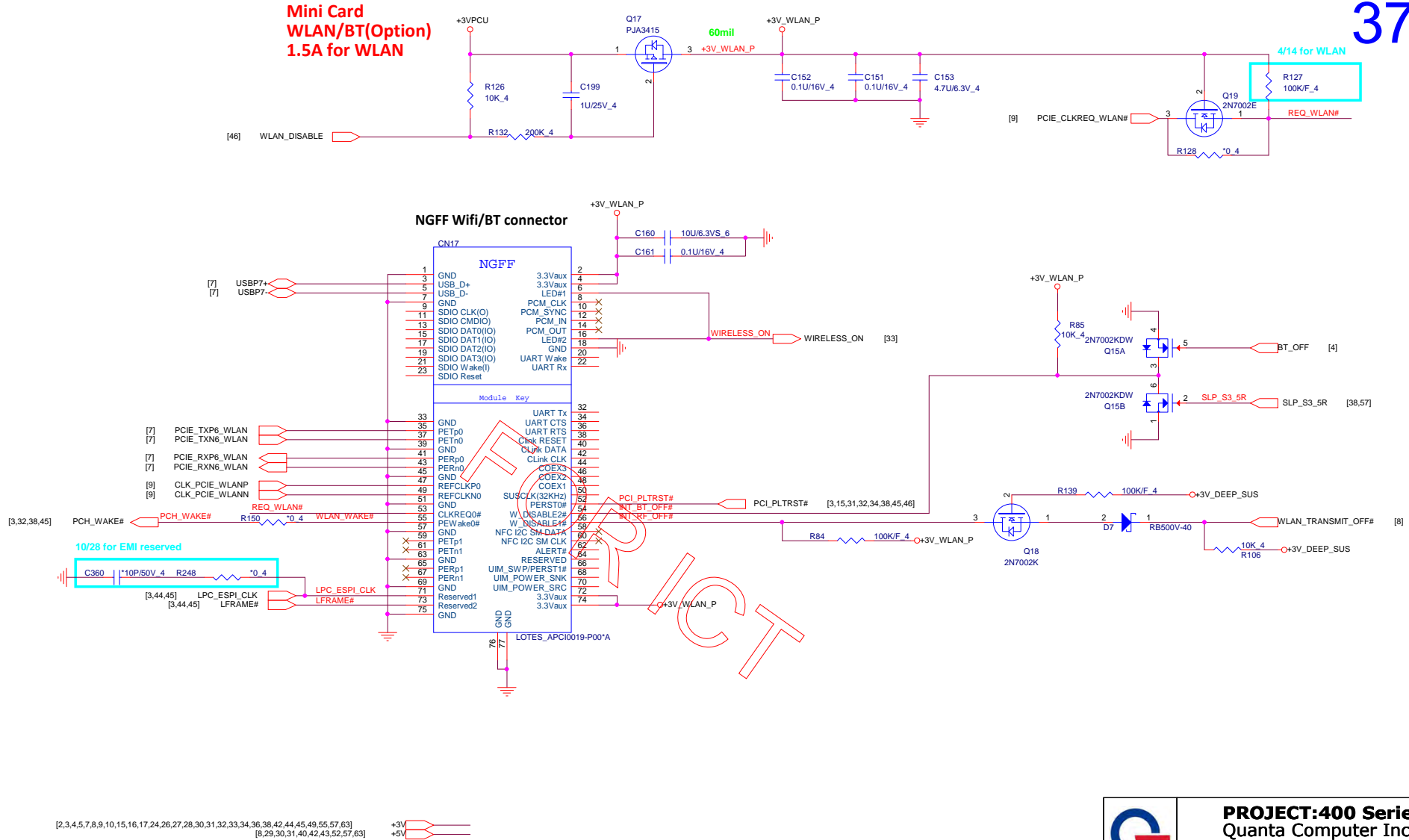
FOR ICT

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,34,38,42,44,45,49,55,57,63] +3V
 [3,10,15,26,33,37,38,40,41,42,44,45,46,48,49,50,51,53,54,57,60,62,63] +3VPCU

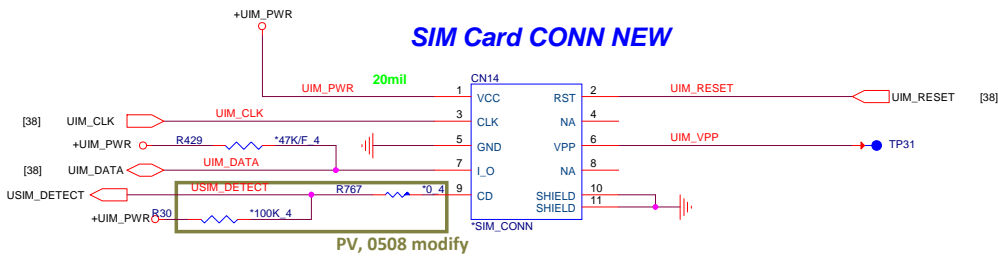
PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 36 -- TS and Accelerometer	Rev 1A
Date: Monday, November 30, 2015		Sheet 36 of 65

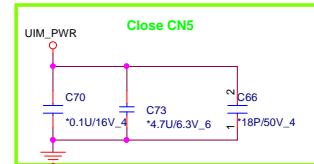
Mini Card
WLAN/BT(Optional)
1.5A for WLAN



SIM Card CONN NEW



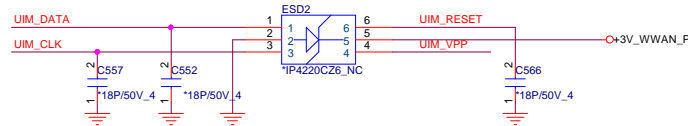
PV, 0508 modify

Trace Length and Routing^u

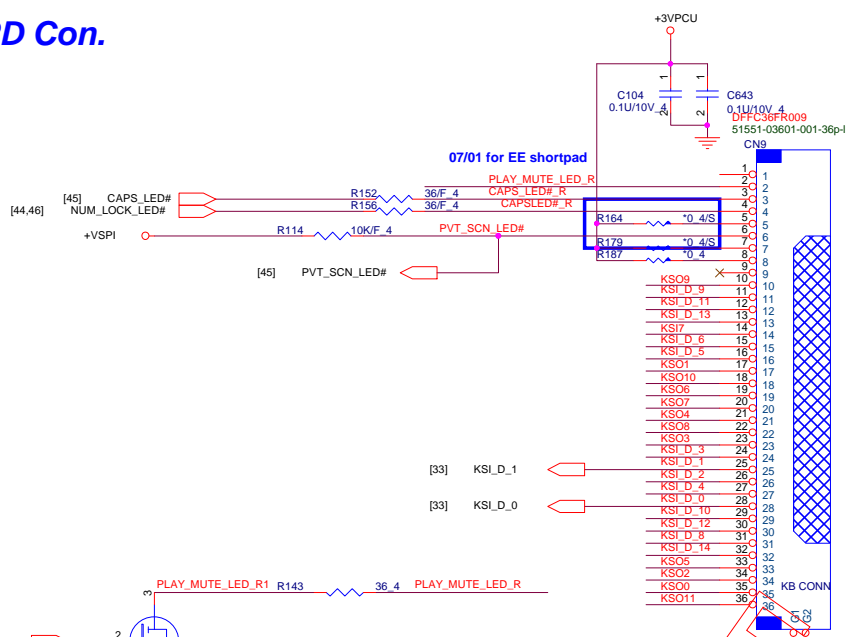
- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.^u
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.^u
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.^u
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.^u

SIM Power^u

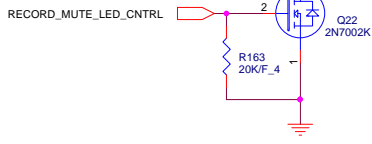
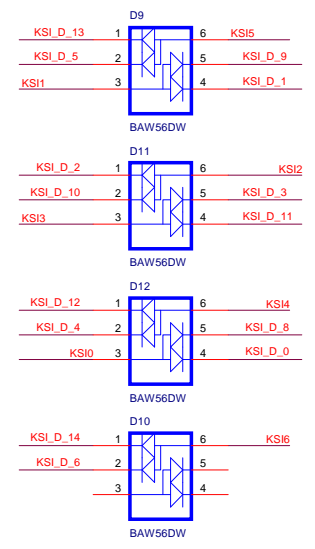
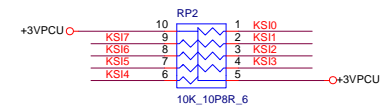
- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.^u
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.^u



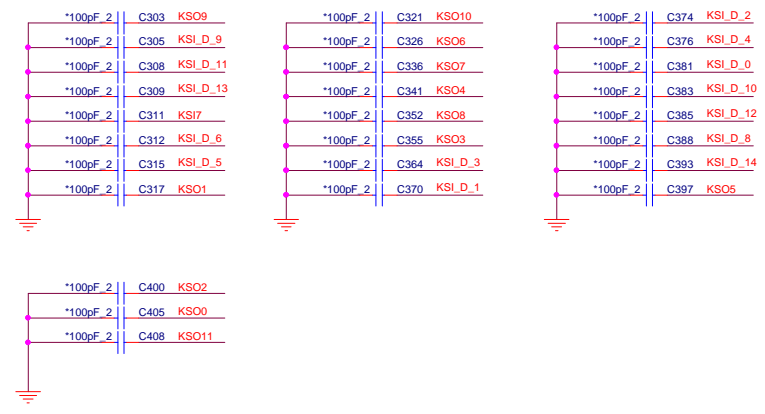
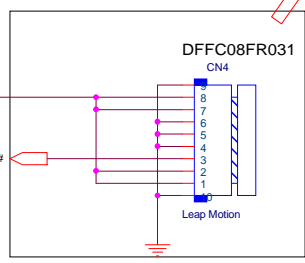
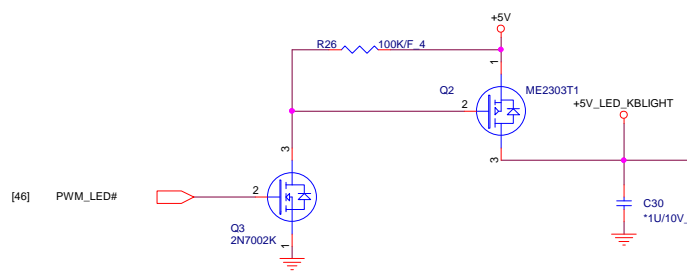
RF cap



KEYBOARD PULL-UP




Need apply PN & FOOTPRINT



[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,34,36,38,42,44,45,49,55,57,63]
[8,29,30,31,42,43,52,57,63]

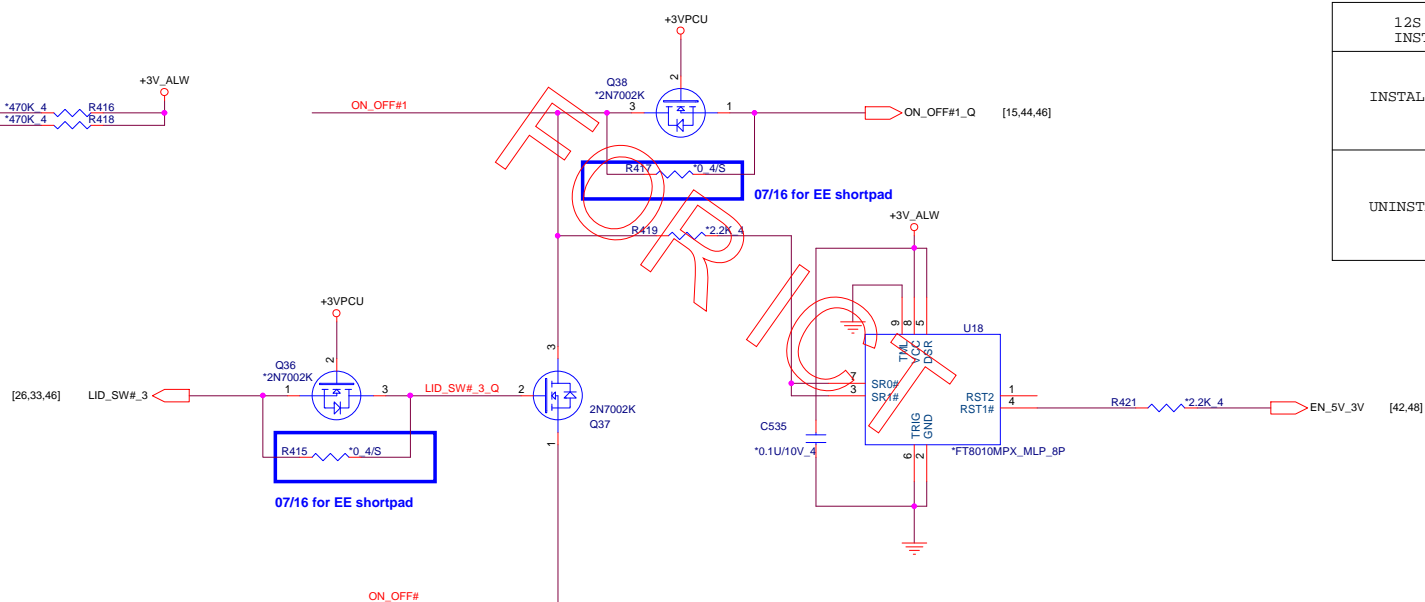
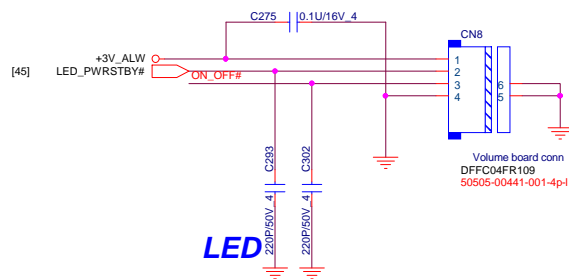




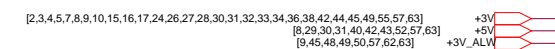
PROJECT:400 Series
Quanta Computer Inc.

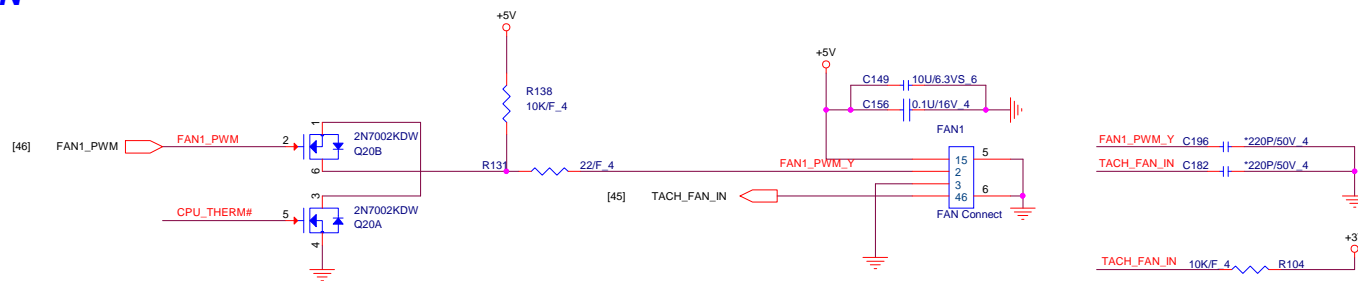
Size Custom	Document Number 40 -- KB/ KB light CONN	Rev 1A
Date: Monday, November 30, 2015		Sheet 40 of 65

Power Botton Connector



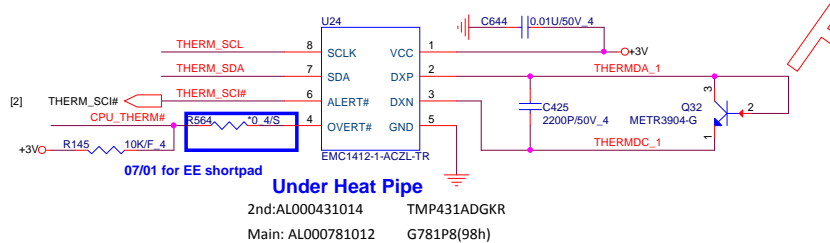
12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R10703 R581 R595
UNINSTAL	R10754 Q7080	R10755 Q7081



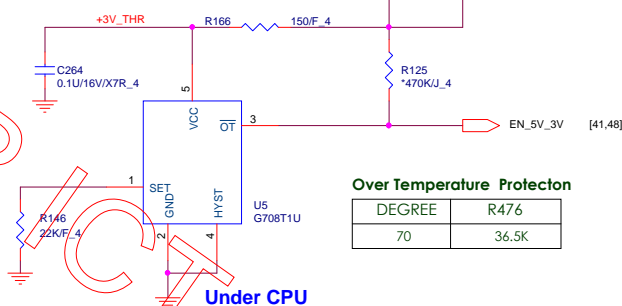


Thermal sensor

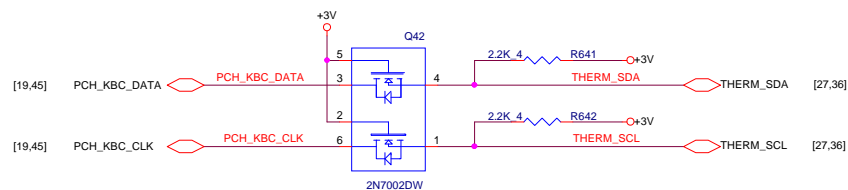
CPU Thermal Sensor



HW protect



$$RSET \text{ (K OHM)} = 0.0012T^2 - 0.9308T + 96.147$$

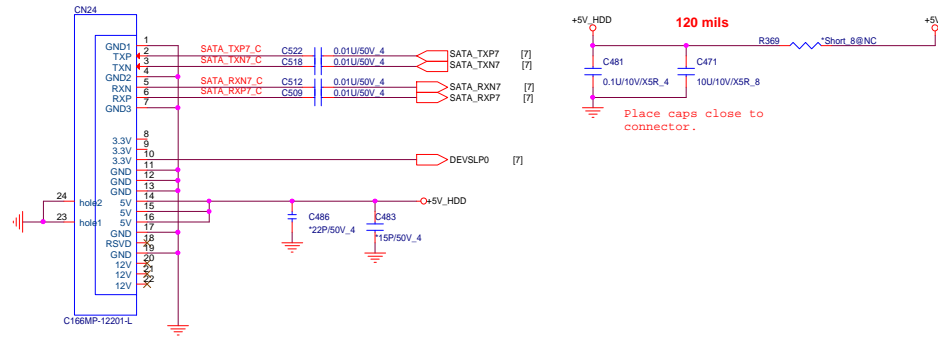


[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,34,36,38,44,45,49,55,57,63]
[9,41,45,48,49,50,57,62,63]

+3V
+3V_ALW

NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 42-- FAN and Thermal IC	Rev 1A
	Date: Monday, November 30, 2015	Sheet 42 of 65	

SATA-HDD



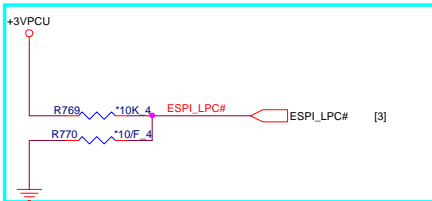
EMI cap

FOR ICT

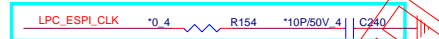
[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,34,36,38,42,44,45,49,55,57,63]
[8,29,30,31,40,42,52,57,63]



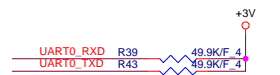
02/10 for Bellagio ESPI



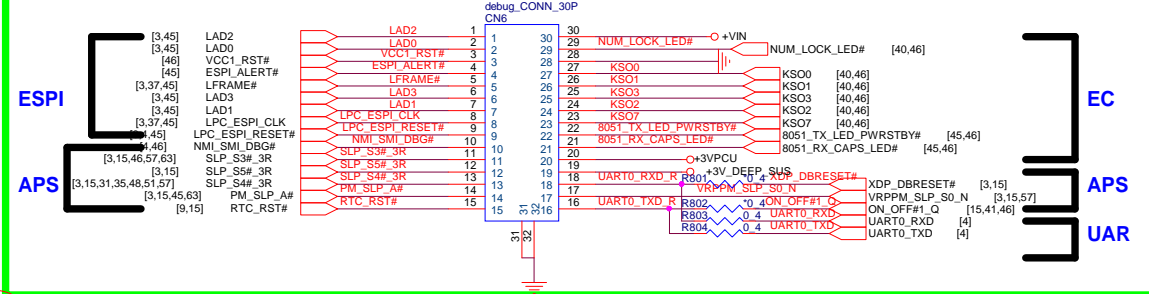
10/28 for EMI reserved



11/04 for check list



ESPI+EC+APS debug conn on MB

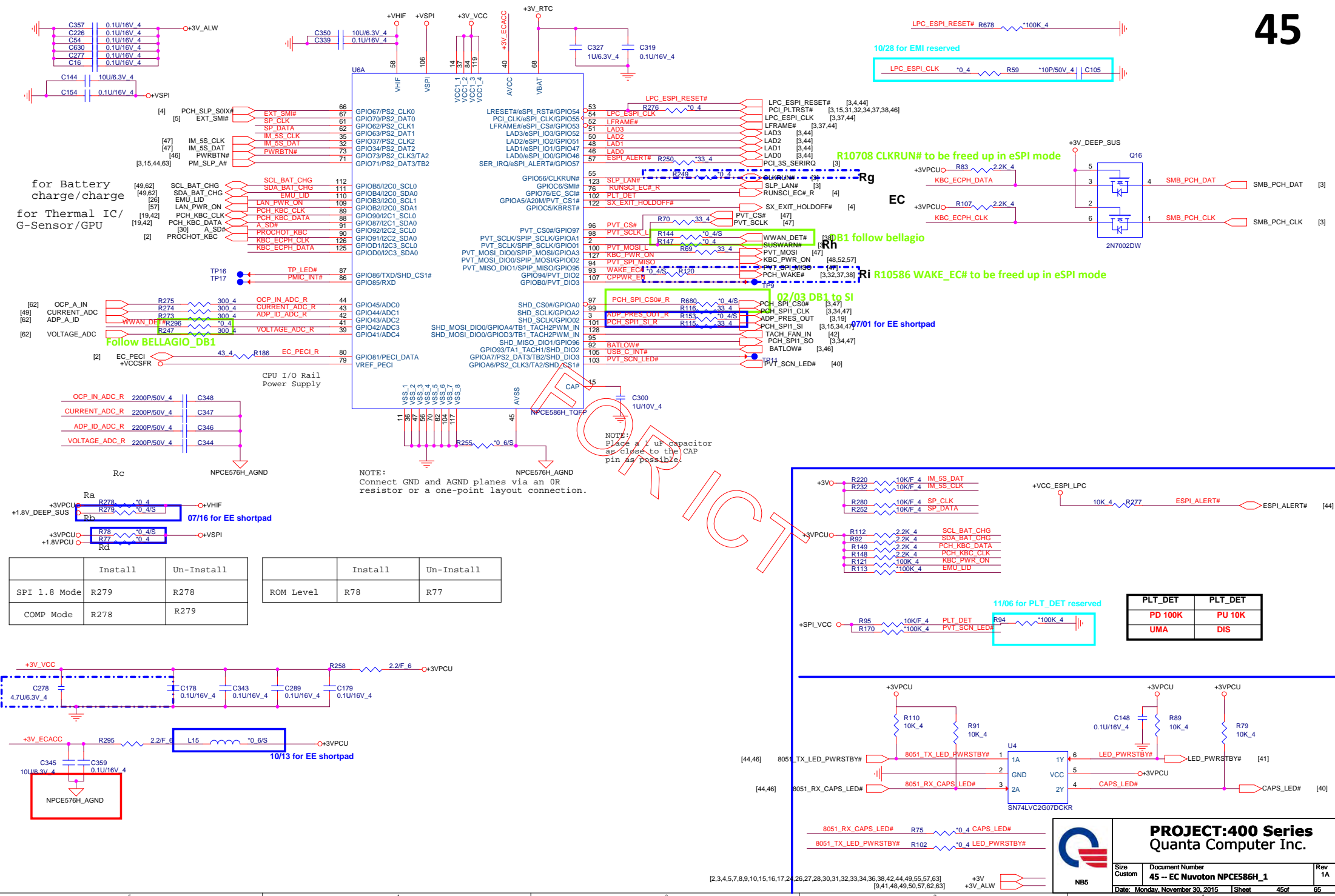


LPC & ESPI TABLE

	LPC MODE	ESPI MODE
R771	INSTAL	UNINSTAL
R769	UNINSTAL	INSTAL
R770	INSTAL	UNINSTAL

LPC & ESPI TABLE

	LPC MODE	ESPI MODE
R658 Ra	INSTAL	UNINSTAL
R646 Rb	INSTAL	UNINSTAL
R659 Rc	INSTAL	UNINSTAL
R656 Rd	INSTAL	UNINSTAL
R649 Re	INSTAL	UNINSTAL
R657 Rf	INSTAL	UNINSTAL
R249 Rg	INSTAL	UNINSTAL
R147 Rh	INSTAL	UNINSTAL
R120 Ri	INSTAL	UNINSTAL
R276 Rj	INSTAL	UNINSTAL
R678 Rk	UNINSTAL	INSTAL



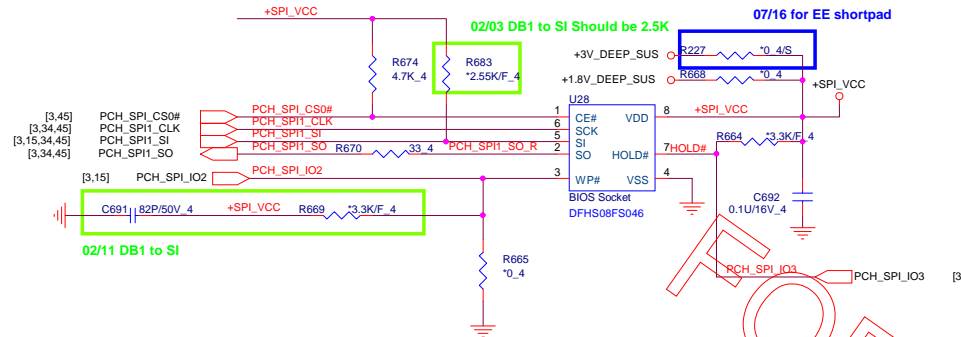
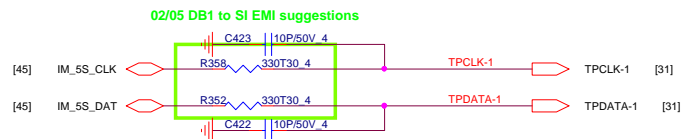
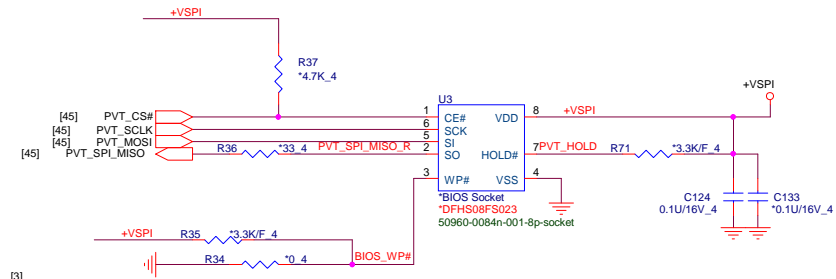
	Install	Un-Install		Install	Un-Install
SPI 1.8 Mode	R279	R278	ROM Level	R78	R77
COMP Mode	R278	R279			

PLT_DET	PLT_DET
PD 100K	PU 10K
UMA	DIS

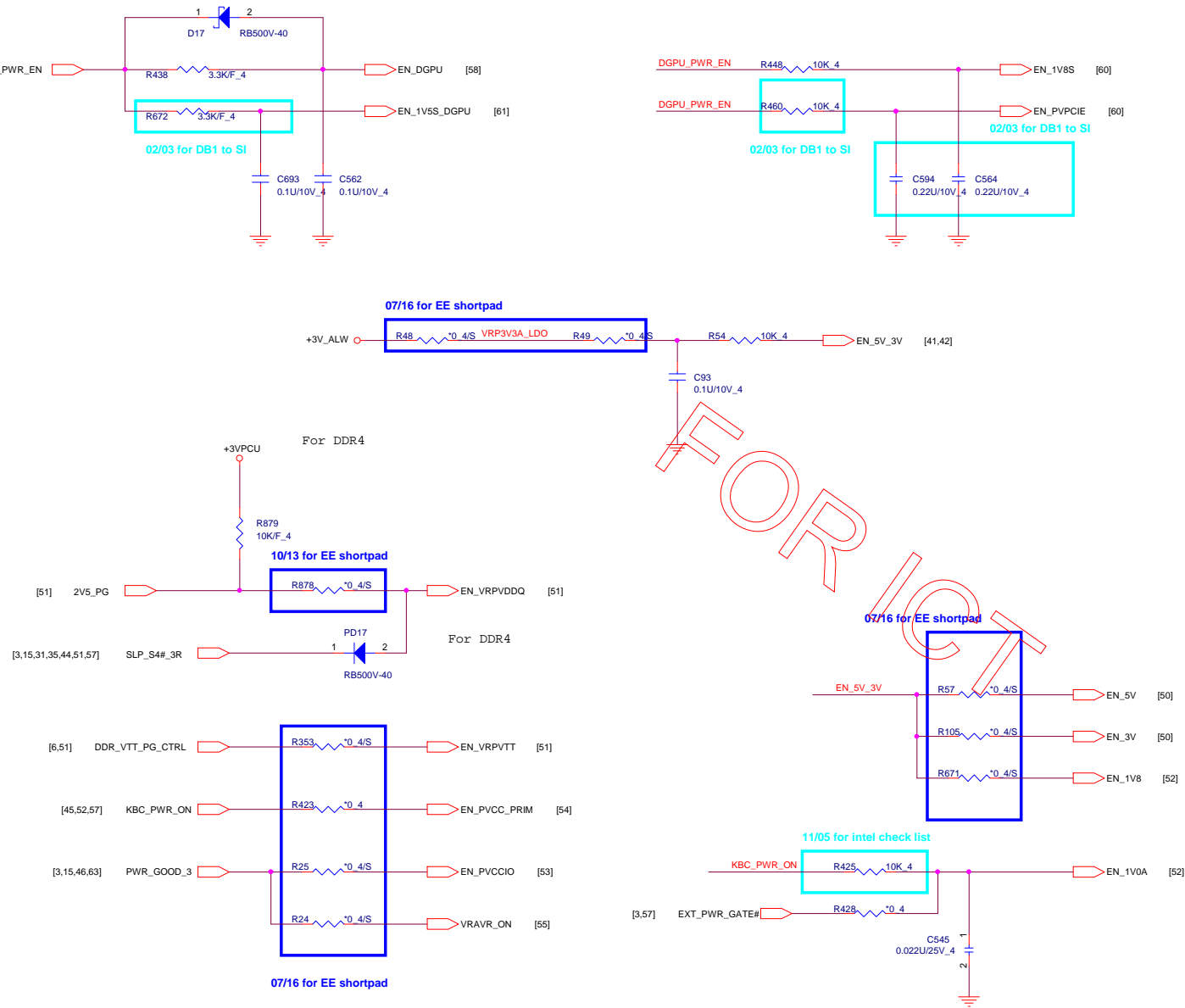
Vender	Size	P/N
Winbond	128MB	AKE3DZN0N01
Socket		DFHS08FS023


Vender	Size	P/N
Winbond	16MB	AKE38FP0N03
Socket		DFHS08FS023

PCH SPI ROM(CLG)

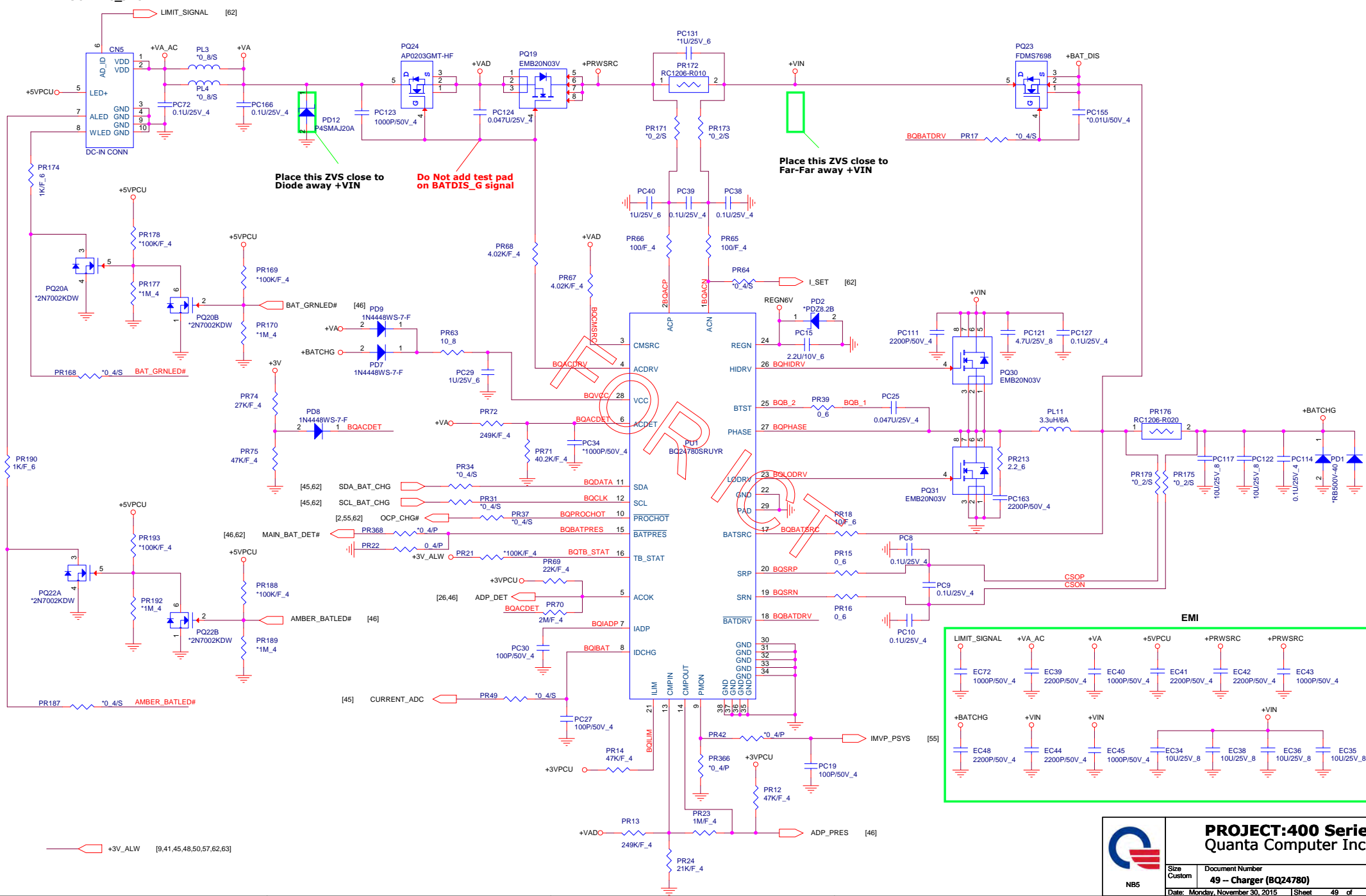
PCH 6*5mm WSON 16M
SPI ROM SocketEC 6*5mm WSON 8M
SPI ROM Socket

POWER TO EE NET NAME CONNECTION

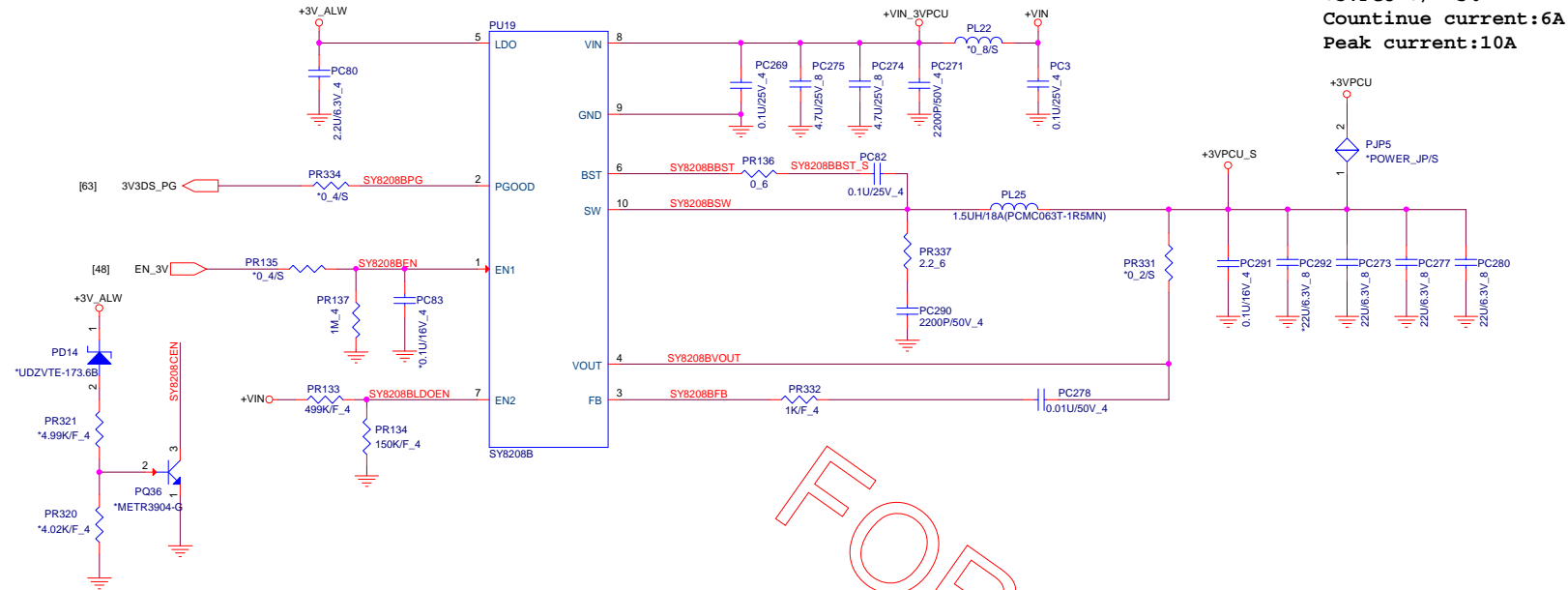


	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 48 -- POWER ENABLE	Rev 1A
	Date: Monday, November 30, 2015	Sheet	48 of 65

90W DC JACK

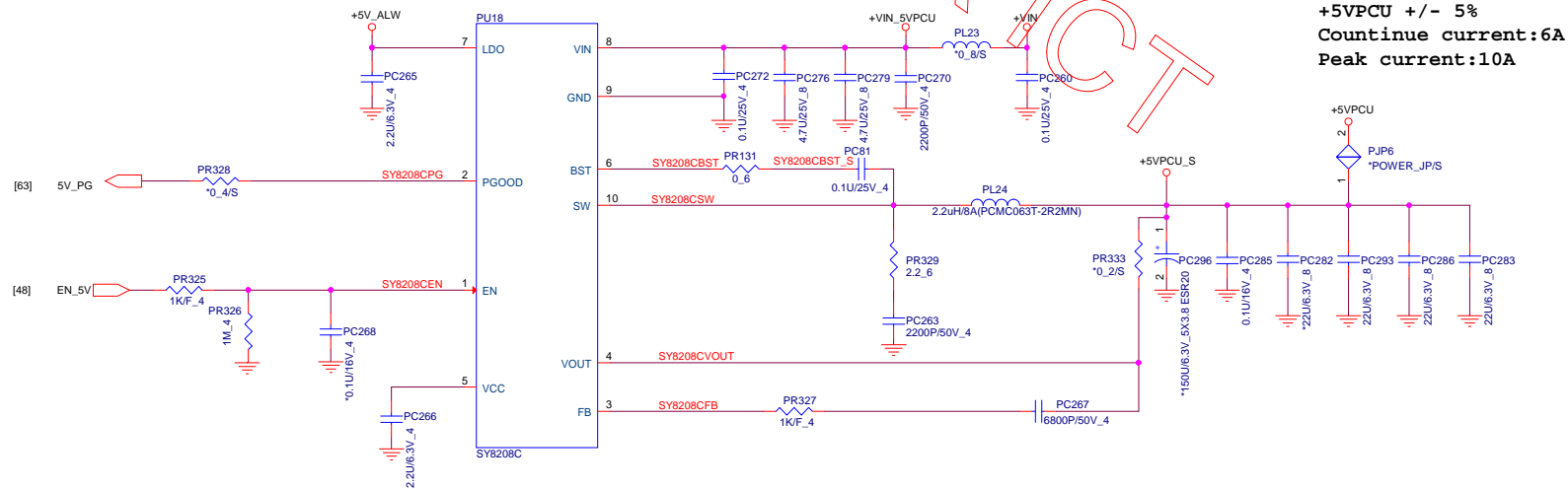



Do Not add test pad
on +3VPCU

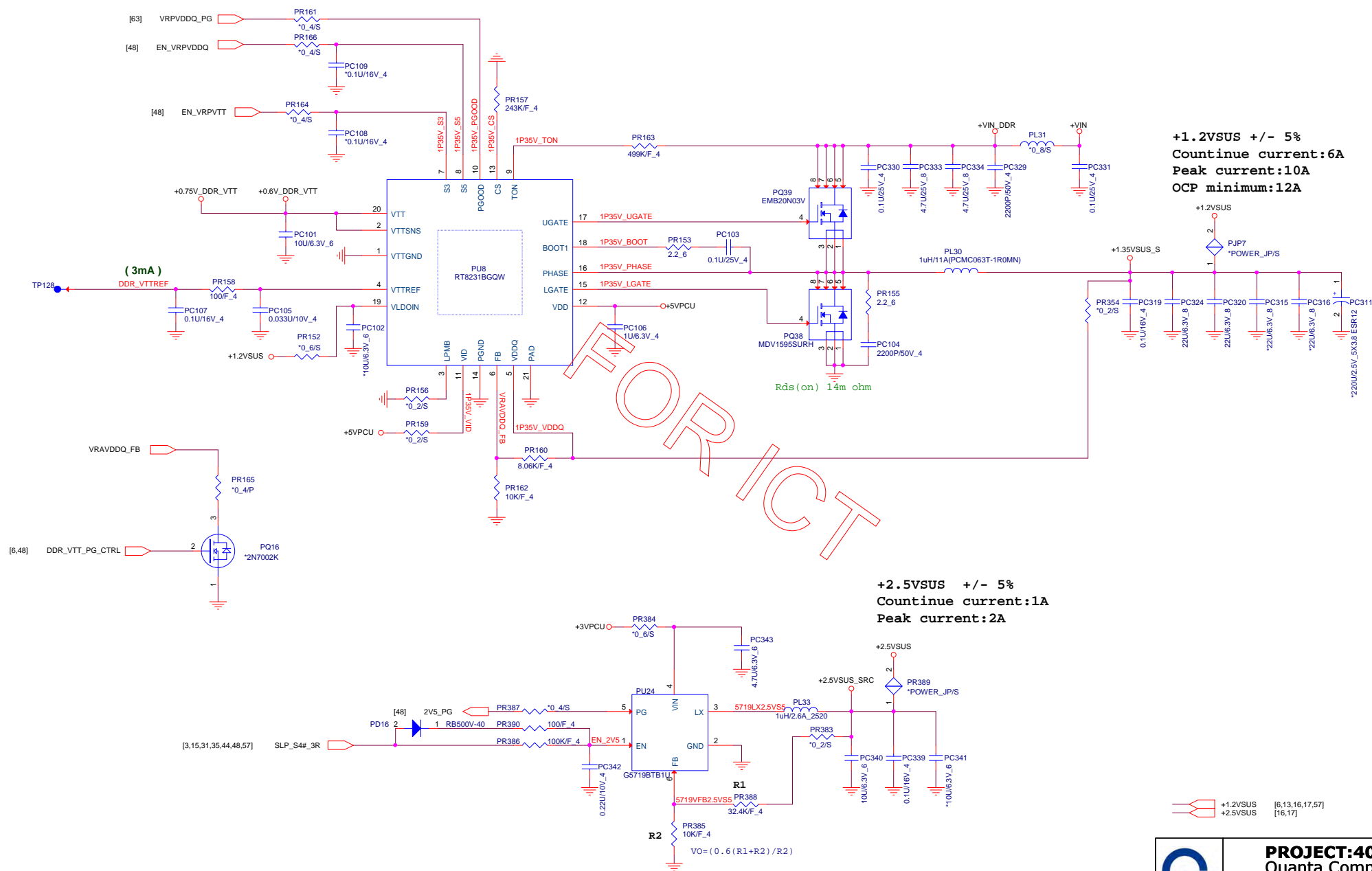


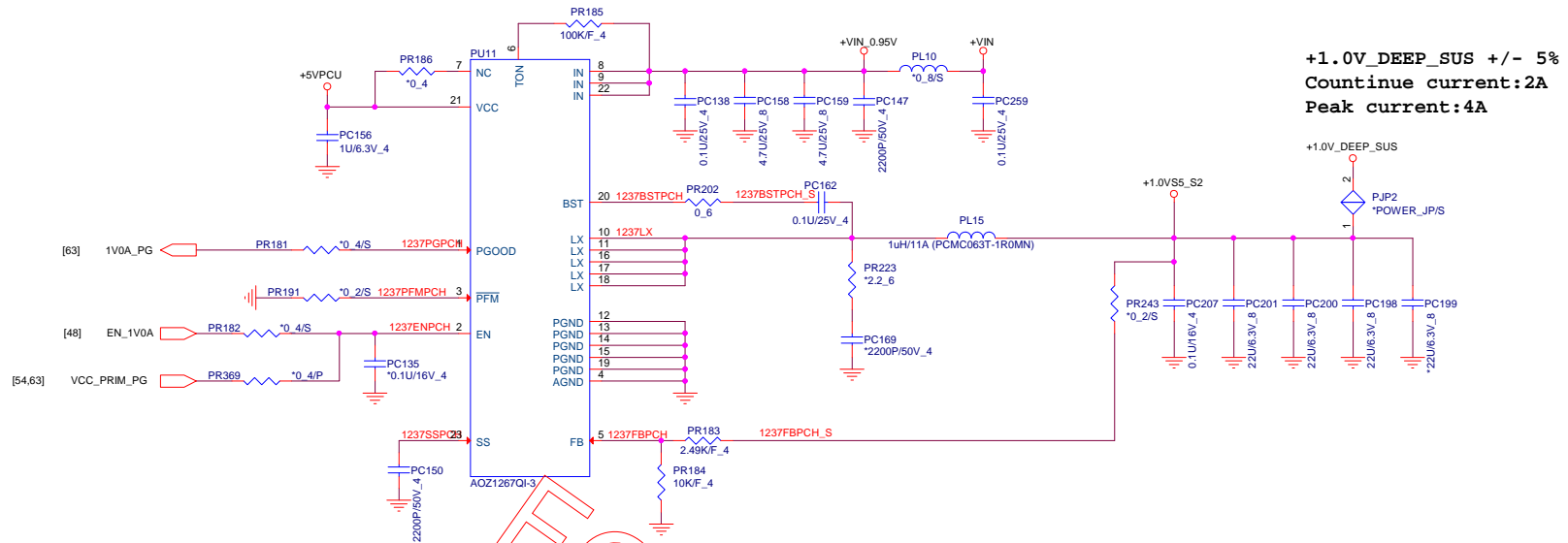
+3VPCU
+5VPCU
[3,10,15,26,33,37,38,40,41,42,44,45,46,48,49,51,53,54,57,60,62,63]
[31,35,49,51,52,55,56,57,58,60,61,63]

Do Not add test pad
on +5VPCU

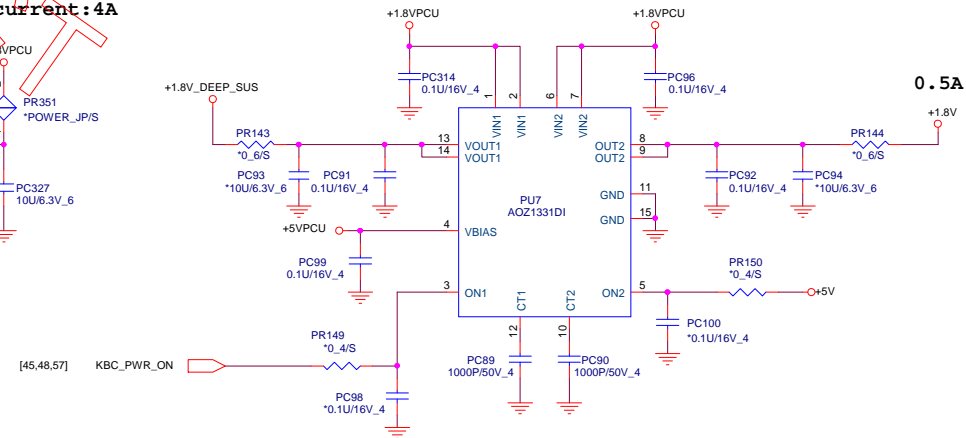
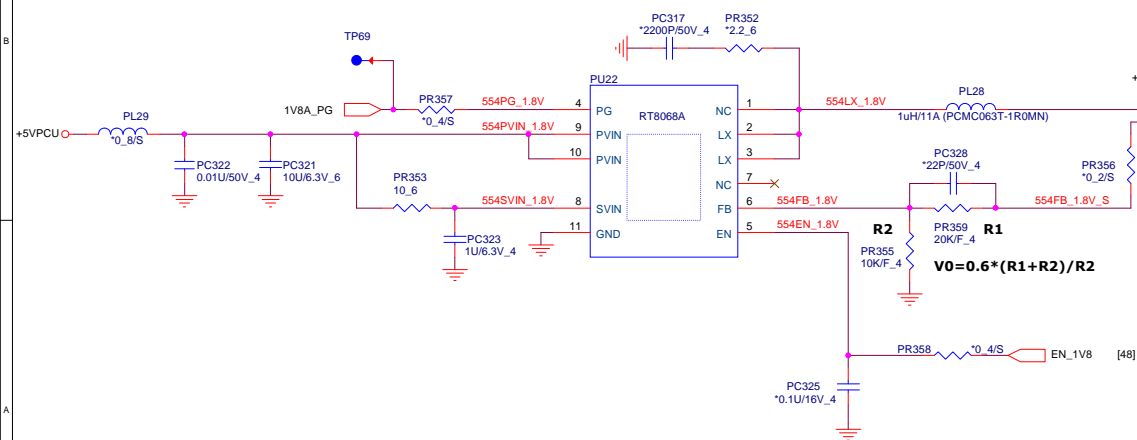


 PROJECT:400 Series Quanta Computer Inc.		
Size	Document Number 50 - 3/5VS5 (SY8208B/SY8208C)	Rev 1A
Date:	Monday, November 30, 2014 Sheet 50 of 65	





+1.8VPCU +/- 5%
Countinue current:2A
Peak current:4A

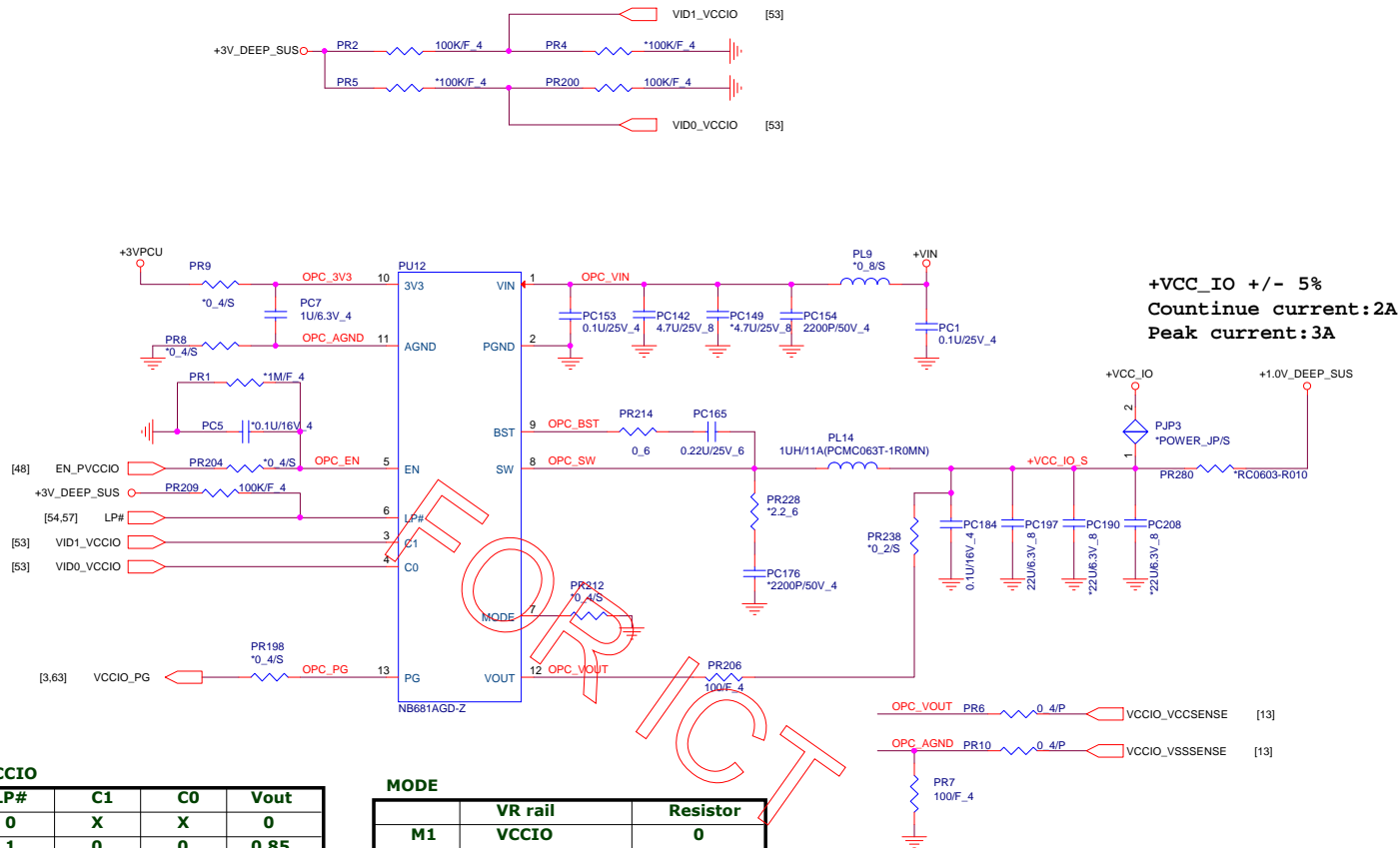


+VIN [25,26,44,49,50,51,53,54,55,56,57,59,61]
+3VPCU [3,10,15,26,33,37,38,40,41,42,44,45,46,48,49,50,51,53,54,57,60,62,63]
+5VPCU [31,35,49,50,51,55,56,57,58,60,61,63]

NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size	Document Number 52 -- +1.0VS5/1.8VS5	Rev 1A
Date:	Monday, November 30, 2014 Sheet 52 of 65		

[25,26,44,49,50,51,52,54,55,56,57,59,61]
[9,41,45,48,49,50,57,62,63]
[5,13,15]

+VIN
+3V_ALW
+VCC_IO

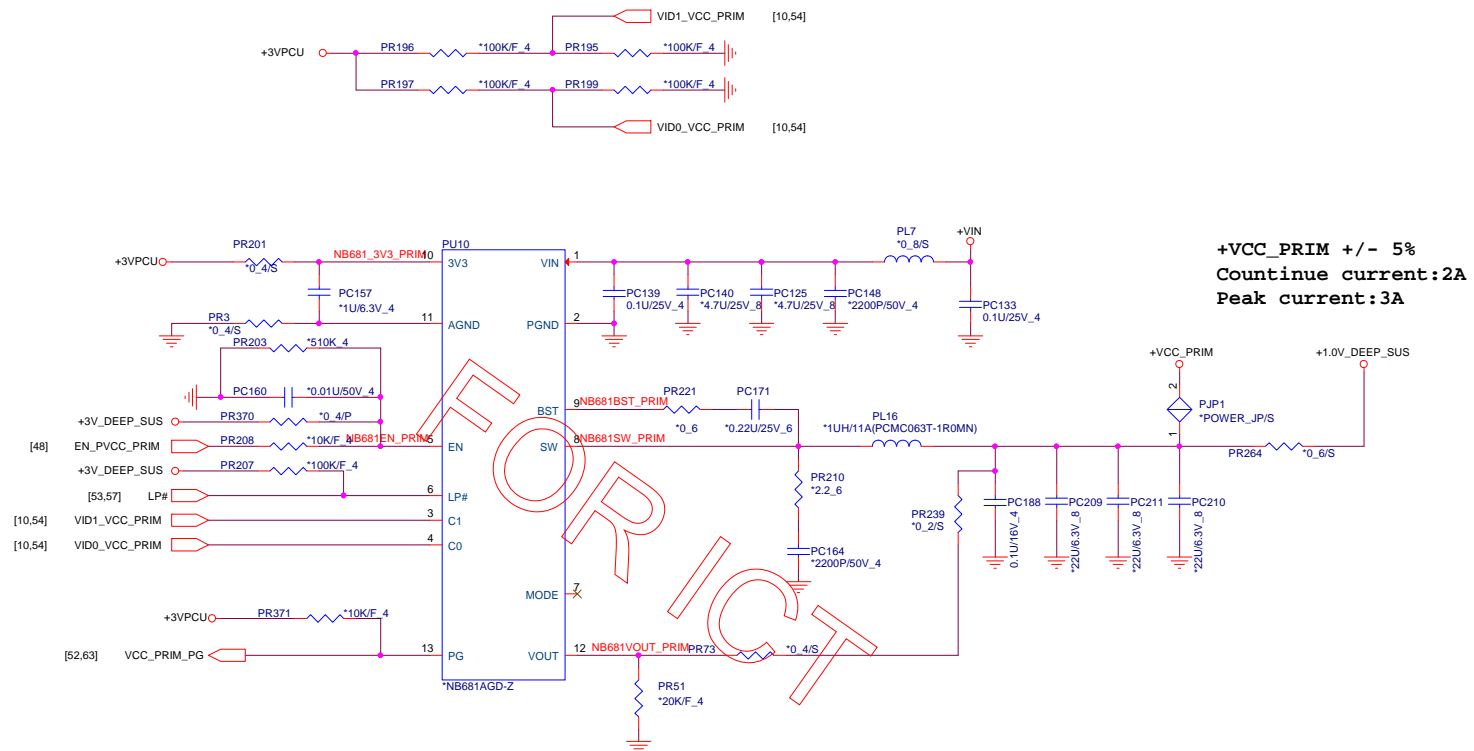


VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

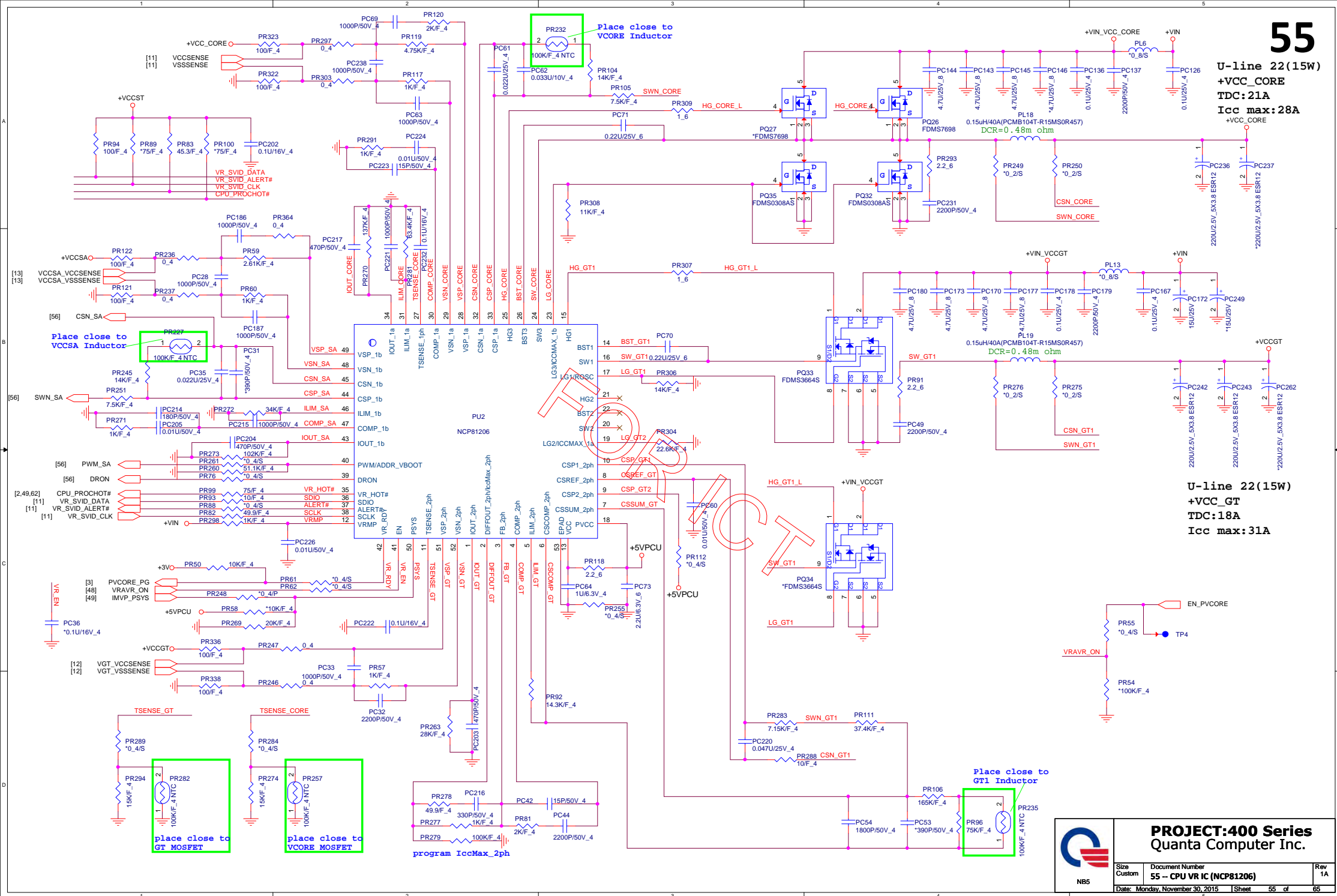


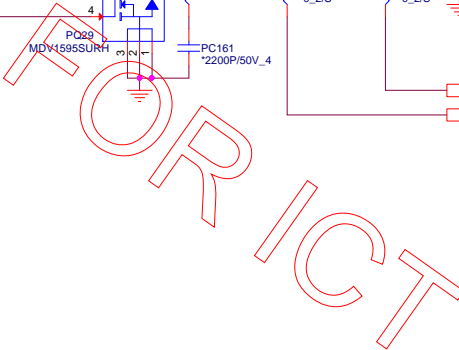
VCC_PRIM


LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.8
1	0	1	0.9
1	1	0	0.95
1	1	1	1.0

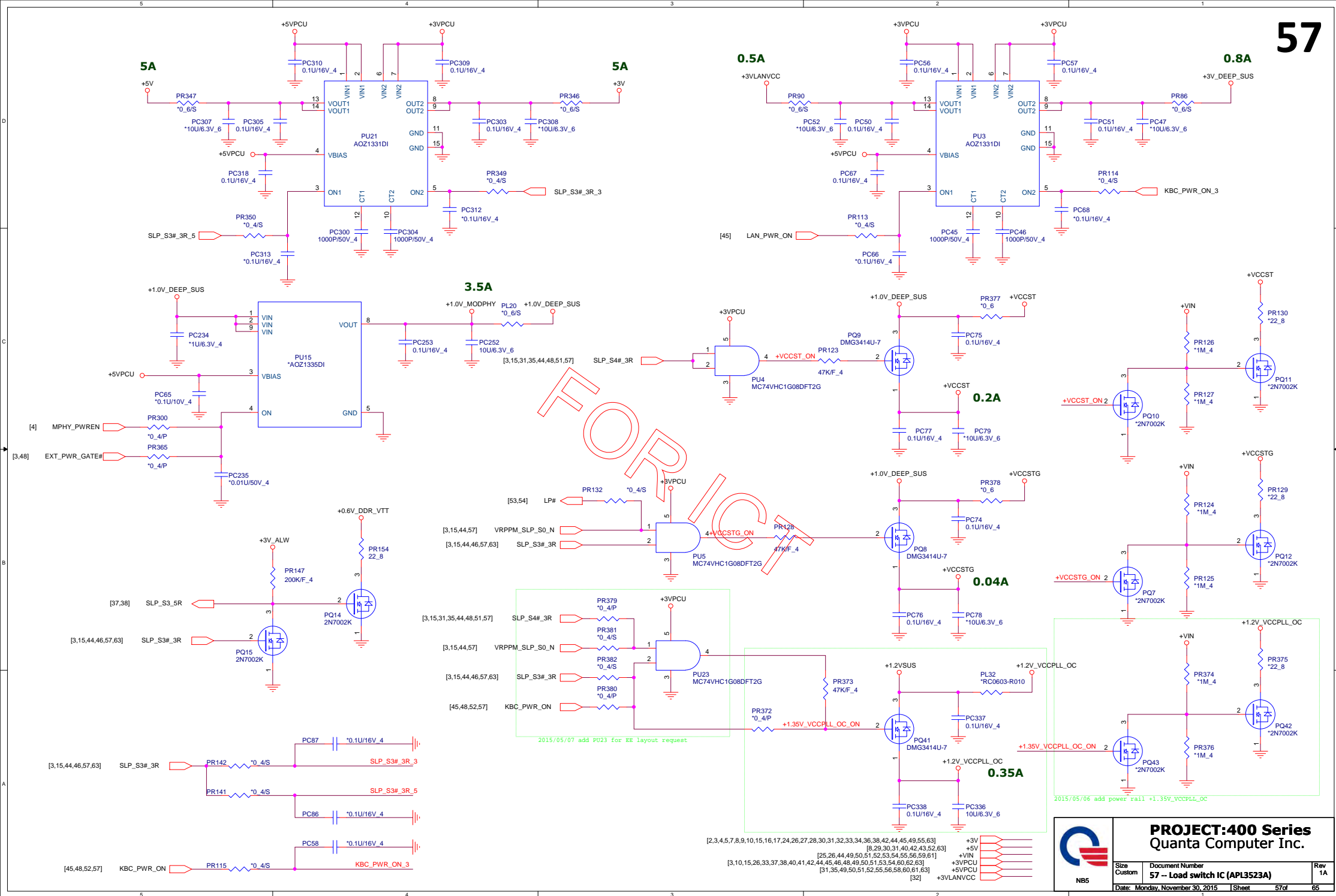
MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EPIO	100K
M4	other	150K



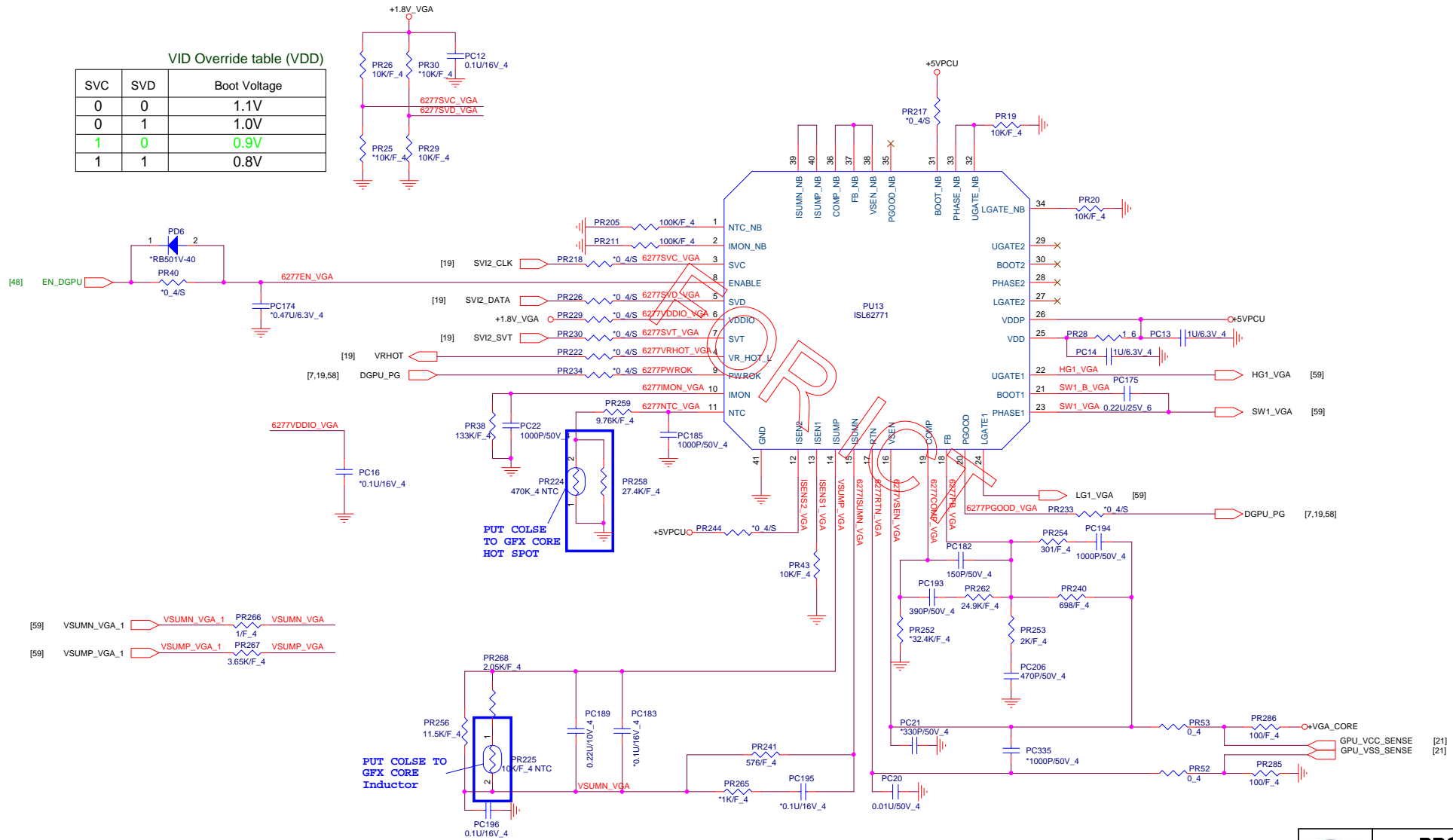


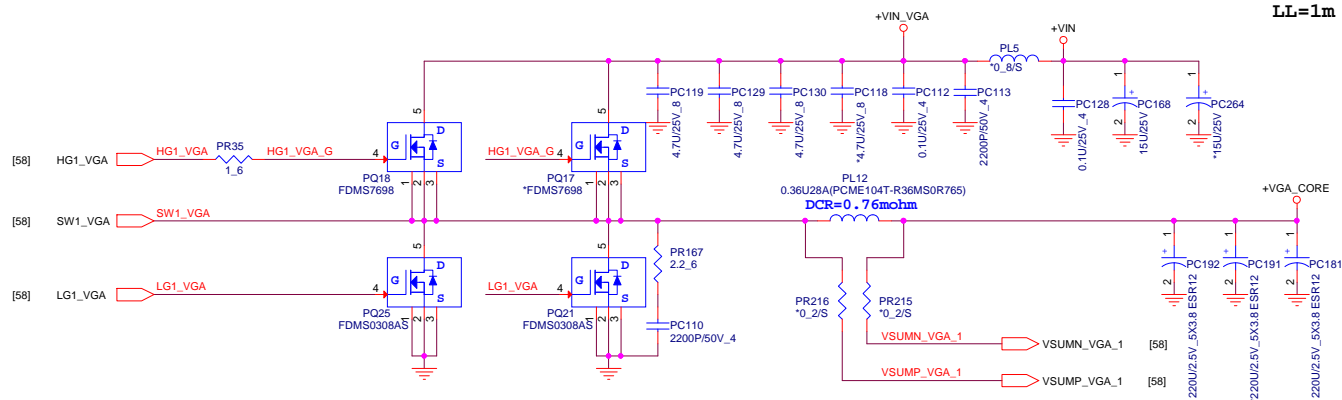
 NB5	<h1>PROJECT:400 Series</h1> <h2>Quanta Computer Inc.</h2>		
	Size Custom Document Number 56 -- +VCCSA (NCP#81253)	Rev 1A	
Date: Monday, November 30, 2015	Sheet	56 of	65



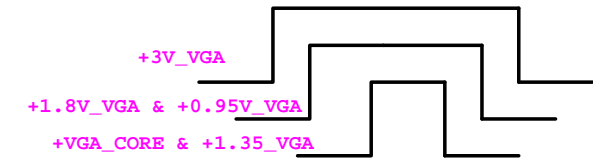
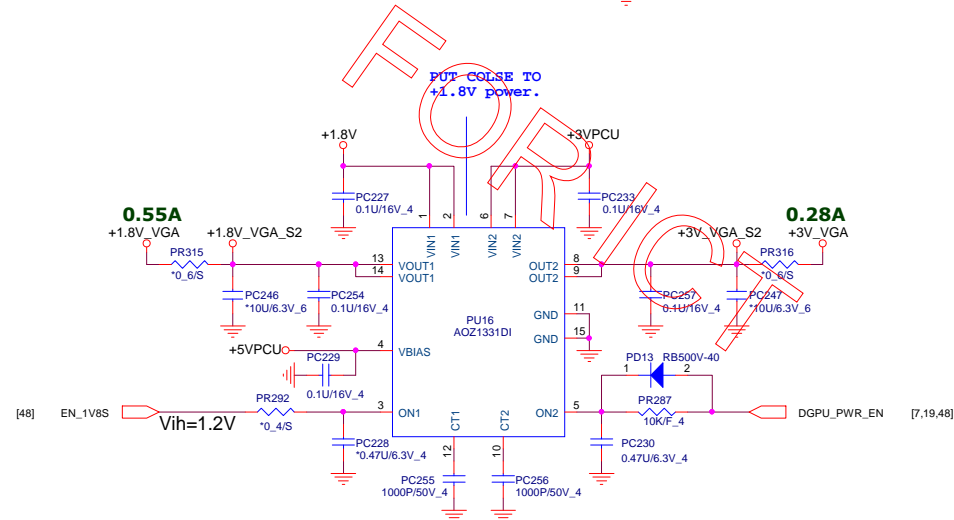
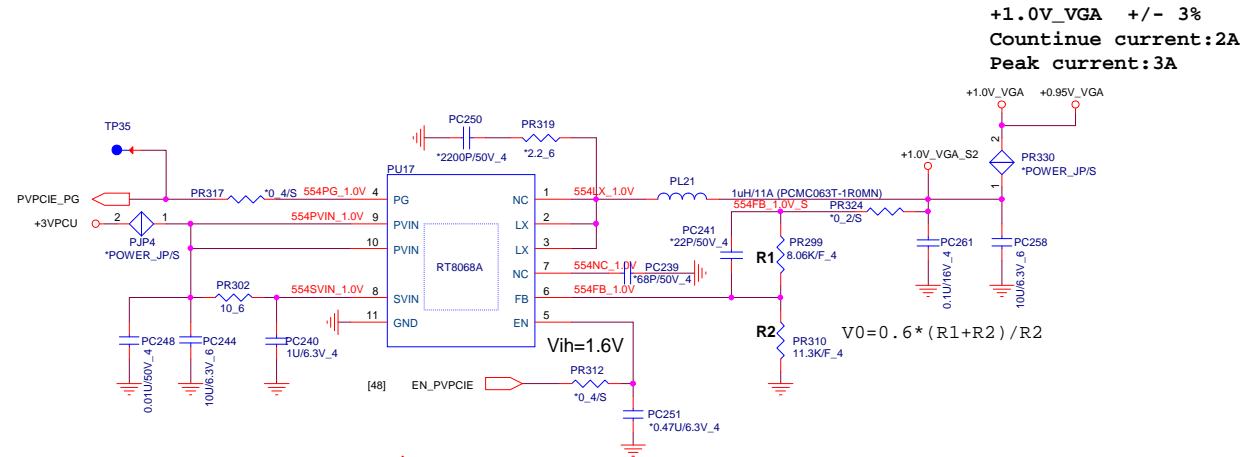
VID Override table (VDD)


SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

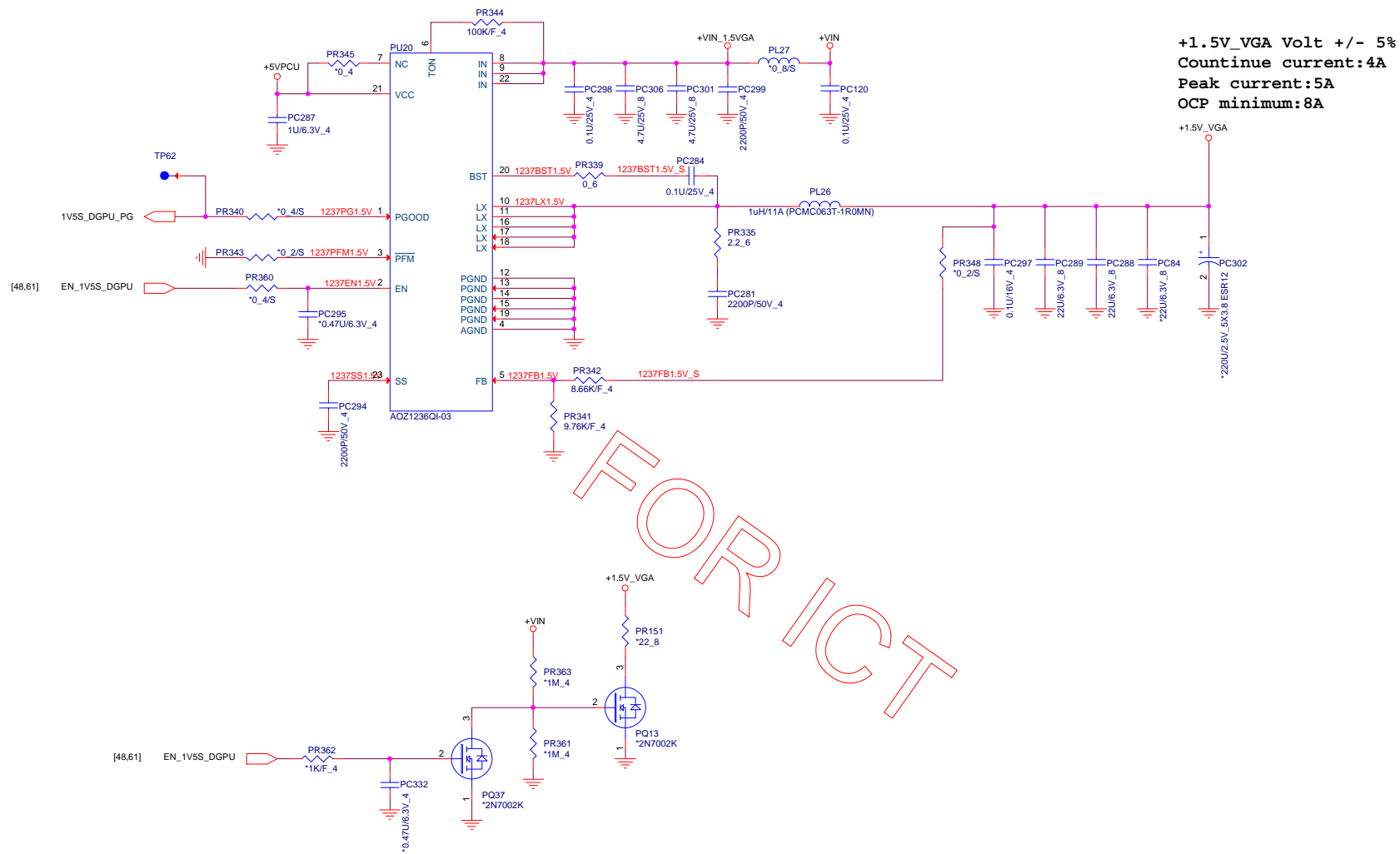




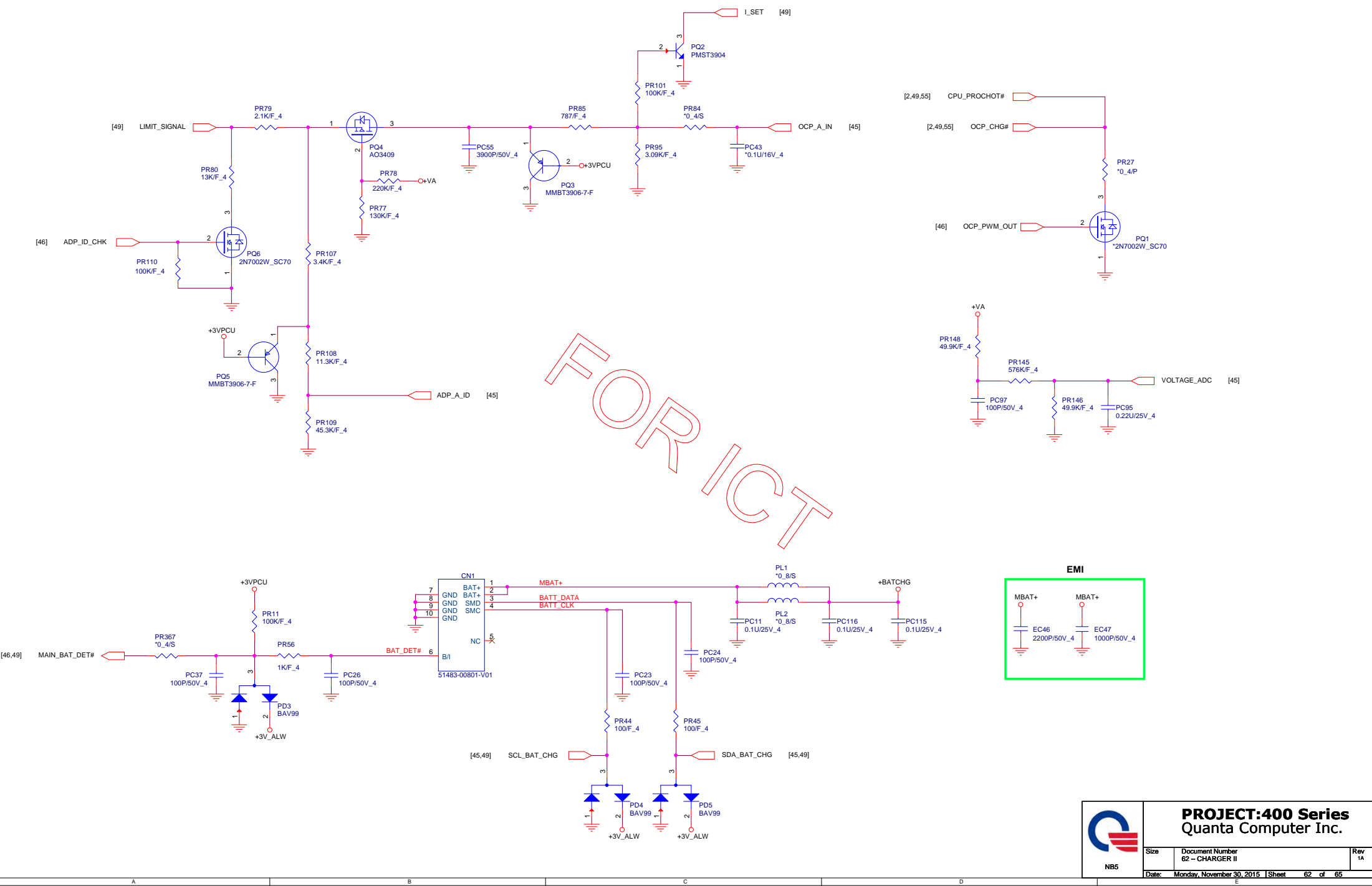
FORICIT



	PROJECT:400 Series		
	Quanta Computer Inc.		
	Size Custom	Document Number 60 -- +1.0V_VGA/1.8V_VGA/3V_VGA	Rev 1A
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Adapter OCP



POK CKT

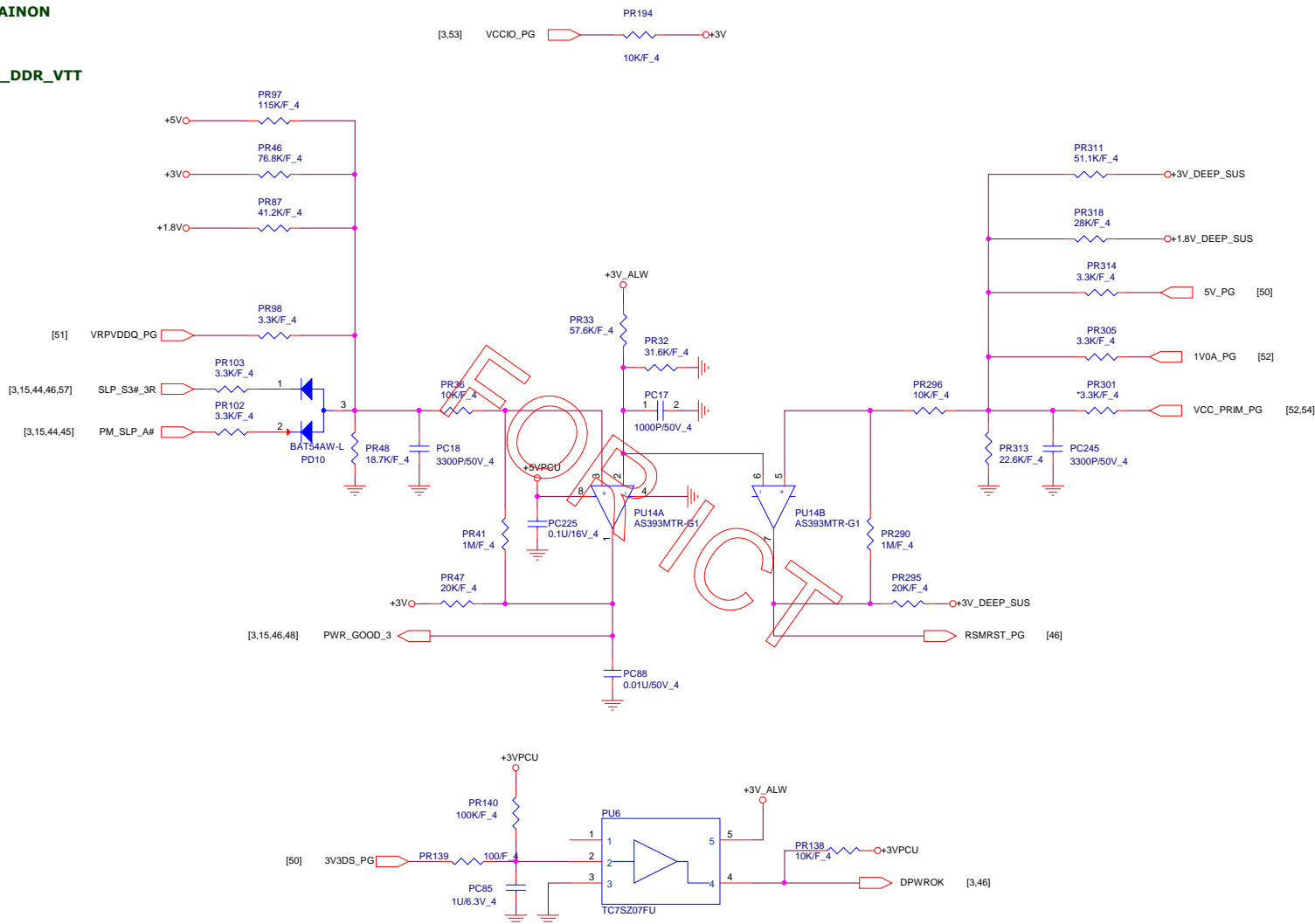
PM_SLP_S4# = SUSON

PM_SLP_S3# = MAINON

+V5S = +5V

+V3S = +3V

+V0.75S = +0.75V_DDR_VTT



[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,34,36,38,42,44,45,49,55,57]

[8,29,30,31,40,42,43,52,57]

[9,41,45,48,49,50,57,62]

+3V

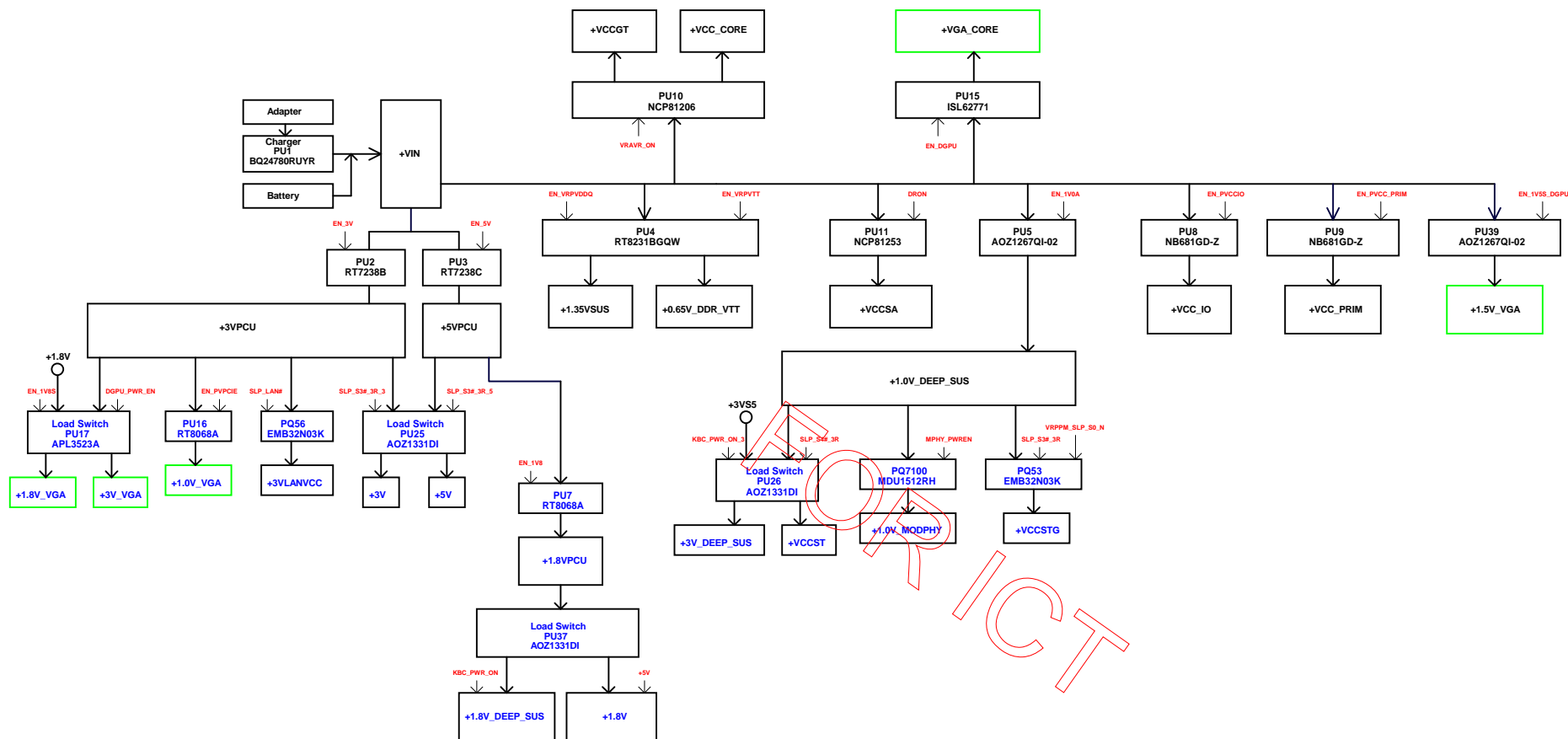
+5V

+3V_ALW

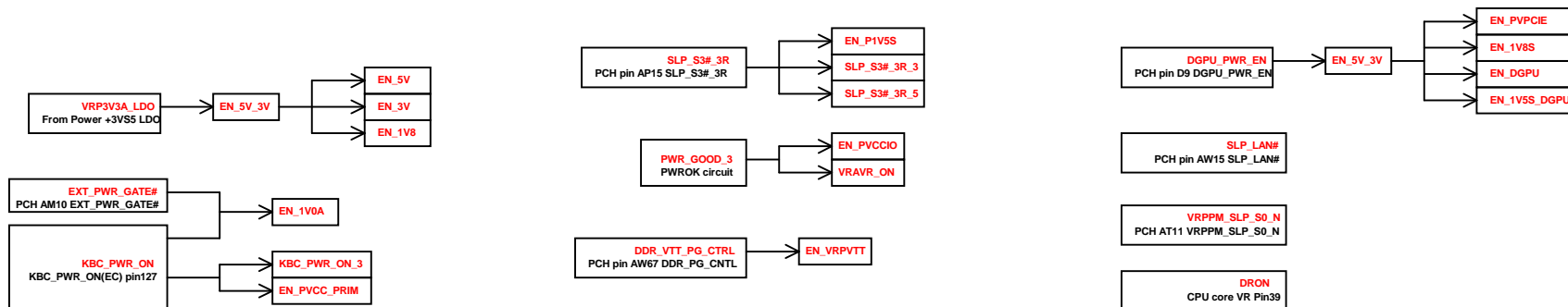


PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	63 - PWROK	1A
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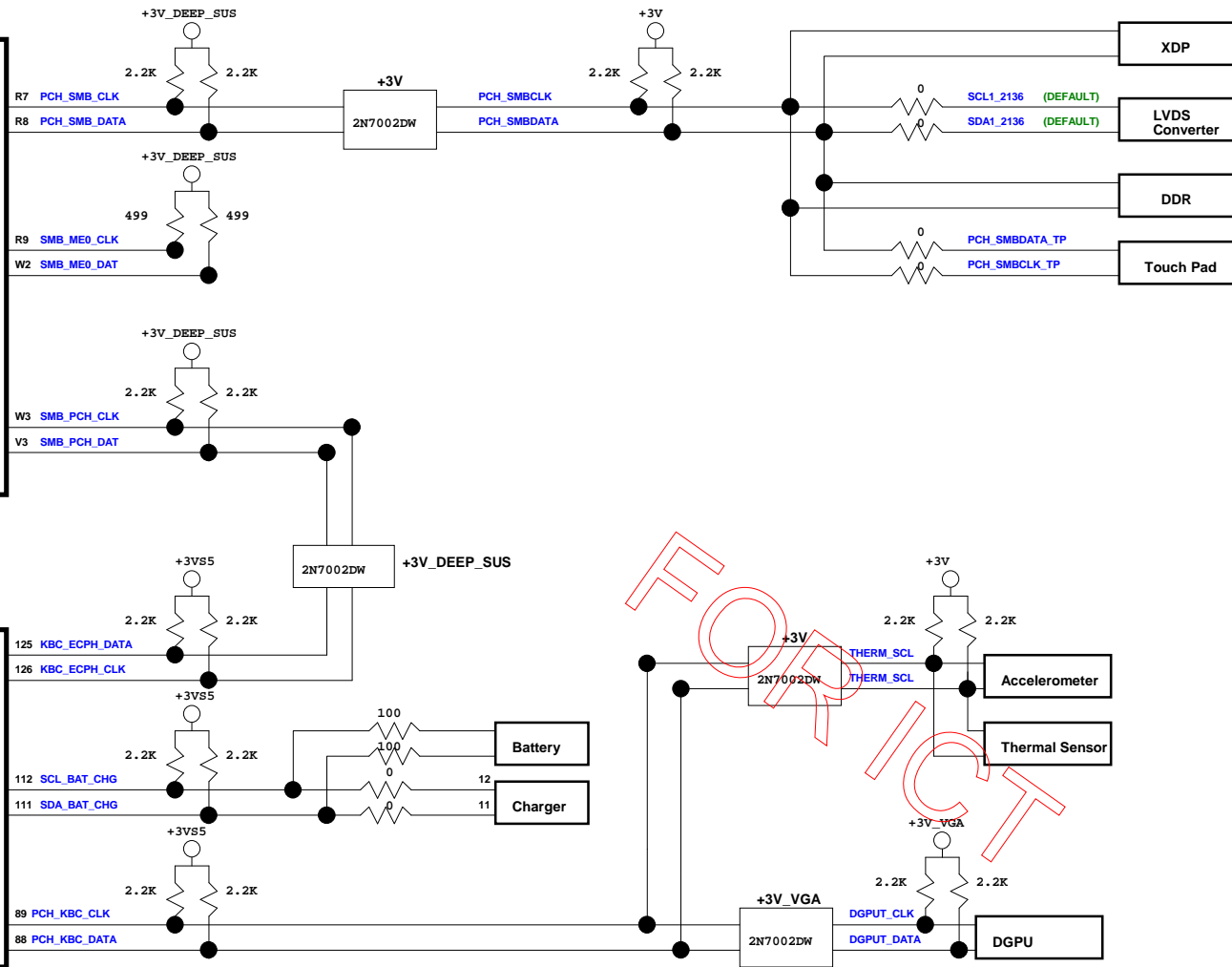


POWER ENABLE PIN



SKYLAKE U

EC
NPCE586H



Example: *499/F_4 and *0_6/S
 * means none-installed
 499 means value
 F means 1%
 _4 means 0402 size
 /S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC